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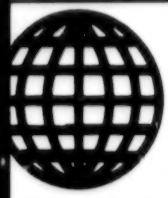

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ADVANCED MATERIALS

New Tungsten Carbide Production Method Noted

90CW0158b Paris L'USINE NOUVELLE/ TECHNOLOGIES in French Feb 90 p 20

[Article by Didier Gout: "Tungsten Carbide: Balls Replace Slabs"; first paragraph is editor's lead]

[Text] The cold-crucible method revolutionizes conversion of tungsten carbide and doubles the life of parts.

Melted tungsten carbide, sold by Technogenia in Annecy in the form of resurfacing cords, is traditionally produced in graphite crucibles. The technique makes it possible to manufacture batches of 10- to 12-kg slabs which are then crushed. The process yielded angular grains of varying shapes whose hardnesses ranged between 1,800 and 2,400 vickers. "The new cold-crucible technique developed with the CNRS (National Scientific Research Center) doubles hardness," explains Gerard Pizzini, Technogenia's production manager. It consists of continuously pouring the mixture of tungsten and carbon to make, not slabs, but balls.

After passing through a small, water-cooled crucible 20 to 30 mm in diameter, the melted carbide stream reaches a rotary dispersion system, where it is scattered into a multitude of droplets 20 microns to 3 mm in diameter. These dimensions allow extremely rapid cooling: temperatures drop from 2,800 to 1,000 degrees C in a few fractions of a second. "The metallurgical structure of the balls is much finer and they are very hard," explains Gerard Pizzini.

The life of parts protected in this way is doubled. This is of particular interest to oil and extractive industries, and in general all industries that use erosion-prone parts protected by melted tungsten carbide. Finally, producers of tungsten balls save energy: with this technique, it is the product to be melted, and not the crucible, that is directly heated through a special arrangement of the induction fields.

Other developments are expected. Technogenia is studying the production of very complex parts using melted tungsten carbide as well as plasma-spray powders with a base of these extra-hard balls coated in nickel.

AEROSPACE, CIVIL AVIATION

ESA Promotes Space Technology Applications

90CW0131A Paris AFP SCIENCES in French 1 Feb 90 p 25

[Article: "Space Technology Transfer Organized by ESA"]

[Text] To facilitate space technology transfer to other sectors of European industry, the European Space Agency (ESA) has chosen a group consisting of the French company Novespace, a subsidiary of the French National Center for Space Research (CNES), the UK company DTE (Defence Technology Enterprise), and the FRG consulting firm MST Aerospace GmbH to serve as the intermediary.

A contract to that end has just been concluded between ESA and the group which will launch a pilot program for space technology transfer to other sectors, expressly for non-space applications. During an initial phase, the Novespace-DTE-MST group will determine which of the most recent technologies are most likely to be usable outside the space sector.

"This research will be done by ESA contractors who will then carry out the transfers themselves or entrust them to the group," states the communique announcing the contract: With the responsibility, in the latter case, of determining the distribution of revenues resulting from transfer agreements.

To reach its objective, the Novespace-DTE-MST group will contact 25,000 non-space companies to determine their technological needs and to offer them the technology to meet those needs, based on the inventory has prepared.

According to Novespace CEO Mr Jean-Pierre Fouquet, there is no question that "the space technologies developed in Europe are numerous and can be applied to other industrial sectors. The claim that technologies are too expensive and only suitable for use under microgravity and ultrahigh vacuum conditions is untrue. Successful and productive examples of technology transfers exist. The ESA initiative will certainly amplify this expertise."

MBB Studies Feasibility of Platform Orbiter

90CW0125A Stuttgart FLUG REVUE in GermanJan 90 pp 78-79

[Article by Goetz Wange: "Is Plato a Hermes Alternative?"; first paragraph is FLUG REVUE introduction]

[Text] The Hermes orbiter is increasingly degenerating into a pure technology program. PLATO, as an unmanned alternative, could limit the risk.

The European orbital glider program is in a difficult phase: Because of weight, the insistence on a crew rescue system has considerably decreased its usefulness. Because the top of the fuselage of the Hermes orbiter will not have hinged payload bay doors like the space shuttle, recovery of satellites or platforms, for example, has become impossible. The greatest effect is on the European Retrievable Carrier (EURECA), which is to be placed in low orbit by the [U.S.] space shuttle next year for the first time with materials experiments on board. It is already obvious that the American transport system will also have to be used by the Europeans for its retrieval. The stronger the criticism of the French Hermes design becomes, the better the chances for a

European Platform Orbiter (PLATO) design, which had already disappeared into the desks of the engineers—because those advising the ESA to imitate the Japanese and obtain their first orbiter experiences with an unmanned vehicle are becoming more numerous.

At MBB-ERNO in Bremen, a PLATO configuration which can be held down to a launch weight of 5,000 kg and therefore launched by either Ariane 4 or 5 has been studied. Like Hermes, PLATO will be mounted on the nose of the rocket which is to place the returnable vehicle in a 500-km-high orbit. The orbiter is designed as a tailless craft which will be controlled by its trailing-edge flaps and its fore vertical rudders. With a wing span of 6.4 m, the orbiter has an overall length of 14.2 m. The angular range of approximately 2,000 km is adequate to take PLATO from a low orbit at a 28.5-degree angle to landing fields in southern Europe. The payload (800 to 1,300 kg) is placed about where the cockpit area for the astronauts is located in the manned Hermes.

With PLATO, Europe could gain the same knowledge, but at significantly lower risk than with Hermes. This would include information about heat shield materials and flight control, tracking, and navigation techniques. Furthermore, with this design, expertise can be gained in reentry and hypersonic aerodynamics, which will be absolutely essential for future manned space transport systems.

Microgravity Tower Experiments Planned in Bremen

90CW0125B Frankfurt/Main FRANKFURTER ZEITUNG/BLICK DURCH DIE WIRTSCHAFT in German 30 Jan 90 p 8

[Article: "First Experiments in Drop Tower in Mid-1990: Bremen Installation Permits Simulation of Weightlessness"]

[Text] Experiments under the conditions of weightlessness, formerly reserved for space flight, are soon to be performed in a 146-m-tall drop tower in Bremen. For the tower, Mannesmann Systems of Duesseldorf planned and installed a 110-meter-long drop tube, which provides a few seconds of true microgravity.

For the Center for Applied Space Technology and Microgravity, ZARM, in the School of Production Technology of the University of Bremen, which is responsible for the tower and the experiments, this constitutes above all a research link between science and industry and opportunities for cooperation between pure and applied research.

With each drop in the drop tower, it is possible to obtain approximately 4.5 seconds of weightlessness in the 110-meter free fall a maximum of 3 times a day. In the area of microgravity, the major emphasis is currently on fluid mechanics. Fluid mechanics aspects of combustion, materials processing technology, and biology will be studied. In space technology, reentry and reentry capsule problems are on the research agenda. The first tests in the Bremen drop tower are planned for mid-1990.

All data emerging from the tests will be recorded by a computer center. High-speed cameras mounted in the drop capsule can record the course of an experiment with up to 6,000 images per second for later on-screen evaluation. According to Mannesmann, the Bremen drop tower is the only facility of this type, at least in Europe.

Aerospatiale's Ionization Process for Composite Hardening

90CW0131B Paris AFP SCIENCES in French 1 Feb 90 pp 34-35

[Article: "Ionization To Treat Composites"]

[Text] The ionization (or irradiation) technique, already used in various fields, from the preservation of foodstuffs to radiosterilization, has just found a new application in the processing of composites used in numerous aviation and space products: airplanes, helicopters, satellites, rockets, and missiles.

In fact, AEROSPATIALE (a monthly publication of the French industrial group of the same name) revealed in its latest issue that researchers at the Aerospatiale-Acquitaine lab have discovered that this technique can also be used in the polymerization of such materials, an operation intended to harden the organic matrix of composites such as glass/resin, Kevlar/resin, and carbon/resin.

Until now, according to the publication, polymerization has been performed using heat in ovens where the materials were heated to temperatures ranging between 120 and 250 degrees C. In the new process, the part being processed is swept by an electron beam, which causes instantaneous interaction between the radiation and the material, with no elevation in temperature.

Ionization thus permits integration of metal elements into the parts because there is virtually no expansion, and the resins are stable over time because they do not include any hardener. Furthermore, ionization is less expensive than heat polymerization and reduces the time required for the process.

The new installation, UNIPOLIS (unit for polymerization by ionization of composite structures), being assembled in the French aerospace group's complex in Acquitaine, will include a 10-meV electron accelerator/20 kw and a 22-m by 12-m chamber enabling processing of parts with a diameter of 4 m and a length of 10 m.

UNIPOLIS will be located in a veritable bunker of 3,500 cubic meters of concrete behind a 300-metric-ton door designed to protect personnel from radiation. The installation, which should be operational in 1991, will be fully automated.

Composites are finding increasingly varied industrial applications because of their light weight, durability, and

heat and radiation resistance. They are used especially in airplane wings, helicopter rotor blades, and missile reentry cones as well as in satellite structures and space launch vehicle shielding.

Italy: Aeritalia, Airbus Sign Collaboration Agreement

90MI0092 Milan ITALIA OGGI in Italian
14 Dec 89 p 11

[Excerpt] Aeritalia is moving closer to the Airbus consortium. Alitalia's acquisition of 20 Airbus-321 twin-engine jets for a total of 1,800 billion lire has opened the door of the European consortium to the Italian aerospace industry.

This was confirmed yesterday by Stuart Iddles, vice president of Airbus Industry, at the signing of the purchase contract with the Italian airline company. He stated: "Aeritalia will construct part of the A-321's body and fuselage. This is the first step toward a broader cooperation with Italy in the future."

The details of the agreement have not yet been finalized because, as Iddles explained, "Aeritalia's supplies are still under negotiation." For the moment, however, the IRI [Institute for the Reconstruction of Industry]-Finmeccanica group's aerospace company will be "a subcontractor for the consortium" and for Iddles "this is an excellent starting point to get to know each other better."

In addition, IRI President Francesco Nobili, underlined that "Alitalia's choice in favor of the A-321 will allow Aeritalia to make a significant contribution to the construction of this type of aircraft."

Iddles was cautious about Italy's possible participation in the Airbus consortium which includes France, UK, the FRG, Spain, and Belgium "given that Aeritalia has always collaborated with the North American competitors."

In fact, Finmeccanica has always worked in tandem with the world's top two producers of commercial aircraft, Boeing and McDonnell Douglas (the Airbus consortium is in third place in the classification). This collaboration first began with the production of fuselage panels for the DC-9 and, later, for McDonnell Douglas' MD-80. However, this step forward in its relations with the European Airbus consortium is part of Aeritalia's development strategy. In 1988 Aeritalia had a 1,655- billion lire turnover and a 68-billion lire profit (a 35 percent increase over 1987). [passage omitted]

Italy: Agusta's Eurofar Project Receives EUREKA Funding

90MI0096 Rome AIR PRESS in Italian
8 Dec 89 p 2327

[Text] Agusta's Eurofar research project has received financial support from the special fund for applied research within the framework of EUREKA [European Research Coordination Agency]. Article 1 of the decree signed by the university and scientific and technological research minister, Antonio Ruberti, on 8 August 1989 and published in the Official Gazzette on 30 November states: "Within the framework of the EU137 EUREKA project and in accordance with the above-mentioned laws, the special fund for applied research shall finance the research activities carried out by Agusta S.p.A. Cascina Costa di Samarate (Varese), classified as a large company, in the form and to the extent indicated.

Location of research: Northern Italy. Research project: EU137—Eurofar (European Future Advanced Rotocraft)—Study for a tilt-rotor aircraft (project IMI 50623). Form of financing: Contribution to costs. Maximum amount: 54,755 billion lire, but not exceeding 50 percent of the allowed costs, to be charged to the quota for northern Italy. Duration: three years and six months, starting from 1 January 1988. Special conditions: Guarantee from Aviofer Breda S.p.A., Rome."

AUTOMOTIVE INDUSTRY

France: Electricity-Powered Car Program Funded

90CW0131C Paris AFP SCIENCES in French
25 Jan 90 pp 2-5

[Article: "1.2 Billion for Research Program on Clean, Energy-Saving Car"]

[Text] Paris—Over the next 8 years, France will devote Fr 1.2 billion to all-out research to create a clean, energy-saving car, according to the 23 January announcement of three ministers (Research, Transportation, and Industry) and the two large French automakers, Peugeot SA and Renault.

A preliminary agreement to that effect was signed that day at the Ecole des Ponts et Chaussees [School of Civil Engineering] by Messrs Hubert Curien, minister of Research and Technology; Roger Fauroux, minister of Industry; a representative of Mr. Michel Delebarre, minister of Public Works, Housing, Transportation & the Sea; and Messrs Raymond Levy and Jacques Calvet, CEO's of Renault and Peugeot.

The decision to launch such a program is the logical consequence of the increase in problems linked to urban pollution, to atmospheric emissions of carbon dioxide and sulfur (greenhouse effect), to the necessity to call a halt to the political mess caused by overconsumption of oil, and to defend, as much as possible, against any new oil crisis, declared Messrs Curien and Fauroux.

The government's share in this program is about one-third (between Fr 450 and 500 million in funding), with the other two-thirds covered by PSA and Renault.

PSA-Renault Clean Car Program

Activities	Expenditures in millions of Fr			Notes
	Joint PSA/ Renault Part	PSA	Renault	
-Clean, energy-saving engine	200	150	150	
ALTERNATIVE SOLUTIONS				Objectives are management of pollutant emissions and consumption as well as reduction of CO2 through reduction in consumption
-Two-stroke engine	75			Objectives are management of pollutant emissions and consumption as well as reduction of CO2 through reduction in consumption
-Alternative fuels	35			
-Batteries	35			
FUTURE SOLUTIONS				Objectives are management of pollutant emissions and consumption as well as reduction of CO2 through reduction in consumption
-Gas turbine	140	70	70	
-Electric highway vehicle	125			
-Use of hydrogen	80			Objective is management of CO2 emissions
-Fuel cells	70			
TOTAL	760	220	220	
GRAND TOTAL	Fr 1,200 million			

Eliminating Pollution

This program is "not intended to provide palliatives for all types of auto emissions, but rather to work on the greatest possible elimination of the causes of automobile pollution," declared Mr Curien during his presentation of the major aspects of the program.

No avenue of research will be neglected: Work will range from basic research in public and semipublic laboratories (National Center for Scientific Research/CNRS, Atomic Energy Commission/CEA, French Petroleum Institute/IFP, National Institute for Transportation and Safety Research/INRETS, the Scientific Engine Group, the French Agency for Energy Management/AFME) to that of the large automakers and to their potential applications.

The research is the continuation of pre-existing cooperation and collaboration. It will deal with combustion, materials, the two-stroke engine, the electric car, batteries, the gas turbine, the use of hydrogen and all other alternative fuels, etc.

This exceptional financial effort, "not insignificant" compared to other European countries, must however be compared to the overall R&D programs of General Motors (Fr 28.4 billion in 1987), Ford (Fr 16.3 billion), Toyota (Fr 10.4 billion), and Fr 3.9 billion for each of the two French automakers.

All the sectors interested in the automobile are involved, not just Peugeot and Renault, emphasized Mr Fauroux. Equipment suppliers—manufacturers of catalytic converters and electronic injection systems, among others—must participate, and the oil companies must not be excluded.

"We have no doubts about our chances for successes resulting from commitment to such a program. Just remember the accomplishments within the framework of the 3-liter project," added the minister of Research, who advocated, as did the other participants, that there ultimately should be research on the European level. "With this program, we are shifting gears," concluded Mr Curien, "because we are tripling the research efforts of the companies in the areas affected."

The research activities, which by now have led to reduction in pollutant emissions from automobile engines, were carried out within the framework of projects targeting reduced fuel consumption or reduced specific emissions of a group of byproducts: carbon monoxide (CO), hydrocarbons, nitrogen oxides (NOx), and particulates. By and large, all the projects have accomplished their objectives. For example, between 1976 and 1988 in France, new car fuel consumption per kilometer was reduced by one-fourth. The fact remains that it seemed "possible and necessary to adopt a more ambitious approach to auto emissions," in the exact words of the text of the program's preliminary agreement.

"Given the advances already made in the area of engines, no new progress can be made without developing a comprehensive approach to the fuel-engine-antipollution treatment system. This approach, which will first concentrate on the private car market, will also involve trucks."

Encouraged and supported by the government, the French automakers therefore decided to combine their efforts:

- to jointly develop a coherent research program
- to gradually and significantly reduce the contribution of auto engines to pollutant emissions.

"The objective is to concentrate on reducing pollution at the source while conserving energy, rather than countering pollution through expensive and energy-hungry treatment."

The point is thus:

- to develop a new approach enabling meeting environmental needs without increasing fuel consumption, especially in urban areas, compared to current vehicles, both gasoline and diesel, and to increase the efficiency of antipollution devices;
- to study promising alternative solutions (new two-stroke engine, engines adapted to new lower-pollution fuels, electric town cars). It is necessary to research avenues permitting significant reductions in the production of CO2 and urban pollution;
- to develop radical solutions (gas turbine, hybrid electric highway vehicle). Other avenues will be explored (use of hydrogen, fuel cells), some of which may ultimately lead to total suppression of CO2 emissions.

As participants in the program, the oil companies will increase the research necessary to produce cleaner fuels.

Research on conventional clean, energy-saving engines will have to "hold their consumption at least as low as that of vehicles produced in 1989, while increasing the reliability and durability of antipollution devices." The 3-year program has a total budget of Fr 500 million, Fr 200 million of which will be provided jointly by Peugeot and Renault, with each of the two automakers adding another Fr 150 million for their individual parts.

The joint part will deal with both the gasoline engine and the diesel engine and will range from the study and modeling of combustion, to the effect of fuels and lubricants on emissions, to optimization of catalytic post-combustion treatment.

The 5-year research program on the two-stroke engine—currently very polluting and very noisy—for which PSA and Renault have provided Fr 75 million should result in the creation of a prototype which satisfies environmental requirements and guarantees dependable, high-quality combustion, etc.

As for the 3-to-5-year research program into alternative fuels for which Peugeot and Renault will commit a total of Fr 35 million, it will deal with oxygenated compounds and natural gas.

Research on the gas turbine will basically continue for 7 years within the framework of the Agata project in the EUREKA program, with the objective of a 100-kW turbine and with a joint French budget of Fr 140 million plus an identical amount contributed 50-50 by the two automakers. In addition to consumption, research will include responsiveness, smoothness, usable fuels (liquid and gaseous hydrocarbons, oxygen, hydrogen), compressors, regenerators, combustion chambers, and materials (high-temperature ceramics up to 2,000 degrees). BMW, Daimler Benz, PSA, Renault, and Volvo are participants in the project along with French, West German, British, Swedish, and Spanish materials specialists.

Research on the electric highway vehicle (5-year preliminary phase followed by a 3-to-4-year specific implementation phase) currently has a budget of Fr 125 million provided by Renault and PSA for the preliminary phase. The objective is the development of a vehicle with an independent range of approximately 500 km, with energy supplied by a low-pollution generator, and with a range of approximately 10 km in town under battery power.

Fr 80 million, for a 4-year initial period, is provided for research into hydrogen as a fuel, lasting a total of 8 years. Issues studied will include the problems of storing the hydrogen in the vehicle (in the form of a hydride, liquid or compressed hydrogen...), of the engine (piston or gas turbine).

Finally, studies of electro-chemical generators, an 8-year program, are divided into research on batteries (Fr 35 million) and fuel cells (Fr 70 million). These deal with improving the characteristics of lead, nickel-cadmium, and sodium-sulfur batteries and determining the best fuel cells for cars.

Peugeot, Renault Reconsidering 2-Stroke Engine

90CW0126A Paris LE MONDE in French
31 Jan 90 p 28

[Article by Annie Kahn: "The Return of the 2-Stroke Engine: Economical, Light, and Soon Less Polluting"; first paragraph is LE MONDE introduction]

[Text] Though simple and inexpensive, the two-stroke engine had one major flaw: It emitted large quantities of exhaust vapors and odors of unburned hydrocarbons. However, thanks to advances in electronics, it could become tomorrow's clean engine.

Already familiar to motorcycle lovers, within a few years the two-stroke engine could well find a position of favor under automobile hoods. Although it currently evokes an image of backfiring and smoke which, to the great displeasure of West German ecologists, accompany the passage of every Trabant, it could become the latest word in low pollution engines.

Most large automakers are devoting a significant part of their R&D budget to it. With a Fr 75-million budget, it has high priority in the "clean car" research program announced last week by the government and the two domestic automakers, PSA [Peugeot] and Renault.

In a four-stroke engine, each cycle develops through four stages. Intake: for intake of the air and gasoline mixture into the cylinder; compression: the piston rises in the cylinder to compress this mixture; explosion: ignition causes an explosion of the mixture, drastically increasing the pressure within the cylinder and pushing the piston downward; exhaust: the piston rises again and forces the burned gases out. In a two-stroke engine, the intake and exhaust stages occur simultaneously. The fresh gases are used to force the burned gases out. Thus, each cycle requires only one back-and-forth movement of the piston in the cylinder rather than two as in the four-stroke engine.

The relative simplicity of the two-stroke engine provides numerous advantages. Superior performance: A three-cylinder two-stroke engine has the same yield as a six-cylinder four-stroke engine. Lower gasoline consumption. Greater power: 50 percent more for a given cylinder, according to Bernard Bertrand, PSA assistant manager of research and scientific affairs.

Service is easier: Oil changes are unnecessary, and it would have 170 fewer parts than a four-stroke engine—which would prolong its service life. It is more compact, 60 percent lighter, and less cumbersome. And finally, it emits less nitrogen oxide into the atmosphere.[1]

So, does this make the four-stroke engine the creation of a mad engineer fanatically devoted to complexity? Certainly not. The disadvantages of the two-stroke engine, although relatively few, are very difficult to overcome. Since the intake of fresh air and gasoline, on the one hand, and the exhaust of the burned gases, on the other, occur simultaneously, it is very difficult to prevent the two from intermingling. But, burned gases remaining in the cylinder interfere with combustion and result in the discharge of unburned gasoline into the atmosphere.

"Very Promising Advances"

The two-stroke engine does reduce nitrogen oxide emissions; however, it increases hydrocarbon emissions. Furthermore, a two-stroke engine requires oil to operate: It consumes 2 percent of oil compared to 0.2 percent for a four-stroke. And finally, it is noisier because the fresh air intakes close violently during exhaust to prevent this fresh air from escaping.

However, "advances in analysis of combustion phenomena, on the one hand, and in electronics, on the other, are very promising for the two-stroke engine," according to Jean-Yves Helmer, PSA automobile division manager.

Advances in modeling in fluid mechanics are, in fact, yielding a better understanding of air currents and of the formation of mixtures as well as the means to overcome the problems. And, thanks to electronic fuel injection, it is possible to wait until the piston has risen and inject the fuel directly into the cylinder after the "ports", i.e., the ducts connecting the top and the bottom of the cylinder, have been blocked by the rising piston.

But, these sophisticated devices are expensive: They could close the current price gap between the two- and the four-stroke engine. The price of the engine represents approximately 10 percent of the price of a car. "Our goal is for it not to be more expensive than a four-stroke engine," states Jean-Yves Helmer.

The Peugeot and Renault research teams, each of which has been performing its own two-stroke engine research, will now join forces. Peugeot had already been working with the French Petroleum Institute and Renault with Modern Engine, a contract research firm.

Engine Designers' Dream

For this new project, a 3-to-5-year initial phase will attempt to determine whether cost-effective, pollution-free operation of a two-stroke engine in an automobile is possible. If the conclusion is positive, the first models will be marketed at the beginning of the 21st century. They will be "deluxe, mid-range vehicles, on the level of the current 309's," believes Jean-Yves Helmer. The total R&D and industrial investment costs will probably be on the order of Fr 3 to 5 billion.

Whereas Peugeot and Renault are the only European automakers interested in the two-stroke engine, it is a different story on the other side of the Atlantic and the Pacific. An Australian, Ralph Sarich, of the firm Orbital Engine, based in Perth, made headlines a few months ago by introducing a two-stroke engine which apparently operates quite similarly to the one being developed by Peugeot and Renault. General Motors and Ford have acquired the patent for it. According to the American journal AUTOMOTIVE NEWS, Orbital is in the process of converting a former General Motors plant in Michigan to produce these engines. They will initially be used for boats, then cars.

The Japanese are also working to improve the two-stroke engine—Toyota, in particular. Its engine, the S-2, operates on a different principle from the two engines above. A compressor exhausts the burned gases.

The two-stroke engine has been somewhat of a recurring dream of engine designers. At Citroen, research began in 1960. And a two-stroke engine nearly became standard equipment on the DS 19. In the United States, Oldsmobile produced a model. That was in 1906. One hundred were sold.

Footnotes

1. The two-stroke engine produces less nitrogen oxide because this quantity is a function of the temperature of the gases: The lower the temperature, the less nitrogen oxide. In a two-stroke engine, exhaust gases remain in the cylinder combining with the fresh gas to augment the mass of gas to be heated. With the same amount of heat, the temperature rises less and thus nitrogen oxide emissions are reduced.

COMPUTERS

France, Israel Plan Joint Supercomputer Project

36980020p Paris AFP SCIENCES in French 1 Feb 90 p 34

[Text] Jerusalem—Arye Shumer, director-general of the Israeli Ministry of Science and Technology, announced on 28 January that Israel and France have agreed on a joint supercomputer project.

Shumer stated that Michael Rabin, professor of computer science at Hebrew University in Jerusalem, and Alain Bensoussan, director of the computer science department of the French MInistry of Research and Technology, agreed to build the supercomputer at a working meeting on 28 January in Jerusalem. Each country will contribute as much as $500,000.

Last May, when French Minister of Research and Technology Hubert Curien visited Israel, the two countries had agreed to develop scientific relations in the fields of computer science and biotechnology.

France: Achievements in Visualizing Supercomputer Data

90CW0128A Paris LE MONDE in French 31 Jan 90 p 32

[Article by Jean-Francois Lacan: "Graphic Display a Source of Discoveries"]

[Text]

An Eye at the End of the Computer

For fifteen years, Jean-Francois Colonna has been helping researchers at the Ecole Polytechnique to visualize supercomputer data. Computer graphics can explore the structure of matter and travel near black holes.

The computer graphics lab is in a windowless, low-ceilinged room on the ground floor of the Ecole Polytechnique. It's hard to make a path through the pile of electronics units and old terminals stacked on makeshift shelves. Lab supervisor Jean-Francois Colonna sits despondently in front of his screen: His Bull DPX 5000 computer has been having serious problems for three days now, and the synthesized clouds that should theoretically be hugging equally artificial mountains are desperately immovable. *"We are terribly low on funds for the continuation of our research,"* he explains, *"and the French equipment we're obligated to buy is taking us out of the running. An image of this type takes about 1 billion operations. American labs produce them in one hour; it takes me a month and a half."*

Just three years ago, though, the Polytechnique lab was a leader in the scientific use of computer graphics, way ahead of its international counterparts. Jean-Francois Colonna was the first to devise the programs and the computer graphics network capable of transforming the work of astrophysics, fluid mechanics, and microphysics researchers. In all these fields, scientists now use supercomputers to analyze or recreate phenomena. But in one hour of calculating, these indispensable machines produce about a billion telephone directories. The interpretation of tens of kilometers of listings becomes a nearly impossible feat.

Jean-Francois Colonna suggested to the Polytechnique researchers that their numerical data be made into graphics in order to visualize the results in near-real time. When this is done, the computer graphics system can provide a representation of the behavior of air masses passing through an aircraft rotor by coloring the data supplied by the computer and following those data as they change over time. The fluid mechanics specialist then has a dynamic model that enables him to immediately pinpoint certain symmetries that would have taken him months to find on paper.

Seeing the Unseeable

While computer graphics helps save considerable time in the interpretation of results, it also makes it possible to see the unseeable, such as the quark structure of matter, where phenomena occur at the speed of light; or to recreate dramatically impossible experiences, such as an observer's view when approaching a black hole in space.

Computer graphics not only grafts an eye onto the ends of the most sophisticated research instruments, it also helps in "casting out nines". Supercomputer programming is a constant source of errors, whether in the mathematical construction of models, the simplification of equations, or the writing of the computer program. Errors that are hard to see on paper, but highly obvious in computer graphics simulations. When the calm swirls representing the circulation of air in a rotor suddenly turn into a sort of stellar explosion on the screen, there is no room for doubt and the fluid mechanics specialists return to their computers to seek out the fatal bug that has slipped into their programs.

Sometimes, the image even has a heuristic function. It can put researchers on the trail of a discovery. Colonna willingly tells the story of a film made to show students the mathematical modelling of the process whereby water diffuses in a solid medium. Looking more closely at the computer graphics images, a researcher suddenly realized that the apparently random progress of the liquid was actually obeying a rigorous logic.

But the image can also be a source of errors. Changing the coloring of certain numerical parameters is sufficient to produce a radically different picture on the screen, leading to interpretations that are diametrically opposed to previous ones. The role of Jean-Francois Colonna and his three co-workers in the computer graphics lab is therefore a particularly difficult one. As mediators between scientific complexity and the actual image, they must faithfully translate researchers' demands while avoiding the pitfalls of representation.

Today, Jean-Francois Colonna is sorry to see his precious 15 years of experience melting like snow in the sunshine. *"We may soon become ineffective due to lack of funds. Every year it's getting harder to obtain an equipment budget. The National Center for Telecommunications Research, our main source of funding along with the Ecole Polytechnique, has abandoned research on synthesized images in order to concentrate on HDTV."*

Neher Lab Integrates LAN, ISDN Technologies

90AN0135 Amsterdam COMPUTABLE in Dutch 24 Nov 89 p 6

[Article by Robbert Hoeffnagel: "Neher Lab Develops LAN-ISDN Integration; Pilot Installation Expected in 1990"]

[Excerpts] Leidschendam—The PTT's Neher Research Laboratory has completed a 3-year study requested by PTT Telecom, resulting in the integration of ISDN and local area network (LAN) technologies. To highlight the possibilities of this "Integrated Services Local Area Network Development" (ISLAND) project, the laboratory has set up a demonstration site. PTT Telecom is still examining whether or not it is going to seek partners for the commercialization of this optical technology.

The ISLAND network demonstrated in Leidschendam consists of two optical ring networks: a high-speed 10-megabit/second basic ring and a 560-Mbit/s overlay ring for broadband applications. The basic ring is a Pronet-10 Token Passing network manufactured by Proteon; the overlay ring has eight 70-Mbit/s channels that are assigned via the basic ring.

The idea behind the two separated rings is that not every workstation has to be connected to the expensive broadband network, since they can be incorporated in the relatively uncomplicated and therefore inexpensive basic network. Those workstations which do require access to broadband services, however, can be included in the overlay network, whose channels are being assigned through the basic ring.

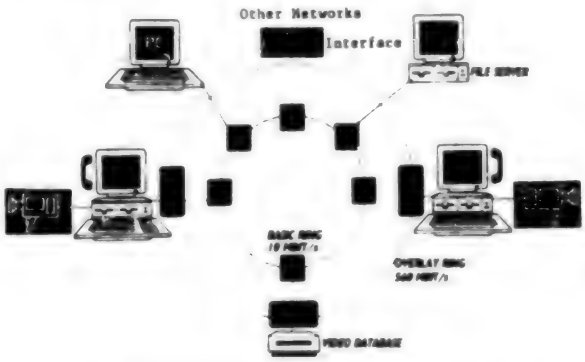
The basic network has a so-called double, star-shaped ring topology (see diagram). This means that although the network is physically structured as a double star network, it still has a logical ring structure. The star topology has been used because of its ease of network extension as well as network reconfiguration in case of any problems.

The overlay ring is a single star-shaped ring. The entire network consists of optical switch gear interconnected by glass fiber cables. The optical to electrical signal conversion occurs in the Fiber Optic Interface (FOI) cards mounted in the workstations. The link to the ISDN services was developed in conjunction with the Technical University of Twente. "InterWorking Units" (IWU) were developed to connect the ISDN terminals to the LAN.

The network can also be hooked up to various external networks, e.g., link to Dataset-1 (X.25) as well as to corporate digital switchboards for 64-kbit/s communications.

Ambiguity

[passage omitted] The Neher lab designed the network on behalf of PTT Telecom's Telematics Systems and Services Business Unit. In the meantime, PTT Telecom has conducted practical tests at its premises which, in its opinion, clearly show that the system can be "perfectly" integrated in a business environment. The Business Unit continues to use the system, which serves as a pilot installation. F.E.A. Willemsen, manager of the Business Unit's Telematics Management Center, expects a first external pilot project to be initiated in 1990. [passage omitted]



The ISLAND System's Network Structure

UK Company Produces Silicon Hard Disk

90AN0129 Paris ELECTRONIQUE HEBDO in French 7 Dec 89 p 22

[Article signed F.G.: "160 MB for First Silicon Hard Disk"]

[Excerpts] The British company Anamartic has made the dream of wafer-scale integration a reality. Its "Wafer Stack" can access eight 150-mm silicon wafers—each one containing 20 MB of DRAM... A "hard" disk that really lives up to its name!

The dream becomes reality at last. Anamartic has just introduced the first memory system based on wafer-scale integration. The module is the size of an 8-inch disk unit and contains eight 150-mm silicon wafers, each one containing 20 megabytes (MB) of memory in the form of a series of interconnected 1-Mbit dynamic random-acess memory (DRAM) chips. This "Wafer Stack" is actually made up of four 40-MB modules—each containing two 150-mm wafers placed face to face—and a control wafer to manage data transfer and storage, as well as the replacement of bad sectors with functional ones if errors occur during operation. The unit is equipped with a small computer systems interface (SCSI) and boasts a typical access time of less than 1 ms; a "native mode" is also available in which access time falls below 200 µs.

The Wafer Stack fills a gap between conventional disk units, which are relatively slow but more densely packed, cheap, and nonvolatile; and the mass storage devices and semiconductor cache-memory systems that are very fast but more expensive. Being volatile, the Wafer Stack cannot claim to replace the former, but rather to complement them, by making data input faster in systems based on the new microprocessors of 30 MHz or more; in theory, it could eliminate wait conditions. Its biggest competitors are the solid-state disks based on card-mounted separately packaged semiconductor memory units. Although it may be a little slower than these, it is less expensive—a factor that could make all the difference. A 40-MB wafer-scale integration module with an SCSI interface should cost about $12,000 (the 160-MB Wafer Stack will cost $28,000), while a solid-state NEC disk with an equivalent capacity is valued at $15,000. The latter has a typical access time of 3 ms (a 20-MB wafer is accessible in 10 µs). [passage omitted]

Commercial Reality

More than its data storage applications, the Wafer Stack's achievement has been to make wafer-scale integration a commercial reality after 20 years of hard, often unsuccessful work. After all, the applications of Anamartic's newly implemented technology are not limited to DRAM's. It can be used with fast static RAM's, in which case access time is even shorter, and the system can be made nonvolatile with the simple addition of a backup battery. The technology is also applicable to other types of circuits, e.g., processors, to create extremely powerful small-size systems (10,000 Mips per 2 dm^2!). Work has been done in this area not only by Anamartic but also by a team of European researchers as part of the European Strategic Program for Research and Development in Information Technologies (ESPRIT).

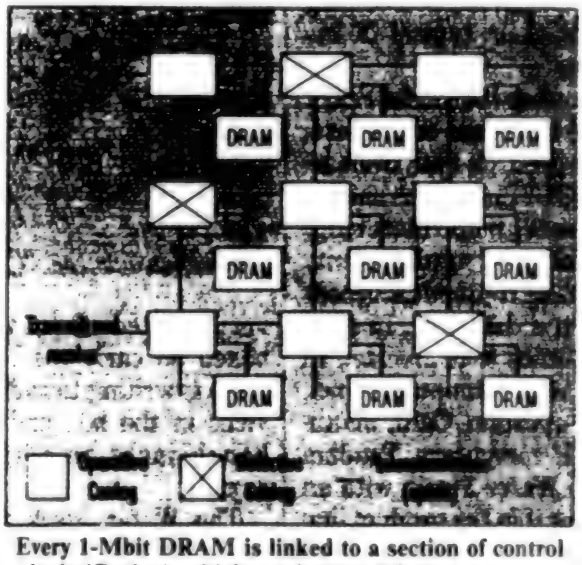
Sample Wafer Stacks have already been tested and evaluated at Tandem Computers, one of Anamartics' shareholders. The U.S. company plans to use them in some of its online transaction processing systems.

Eighty Percent of Bits Usable

An Anamartic wafer is made up of a network of 1-Mbit DRAM memory chips that have been modified to incorporate a section of programmable control logic that Anamartic calls "Conlog"—for Configuration Logic—plus redundant memory cells. This wafer-scale integration technique was described at the 1989 International Solid-State Circuits Conference (ISSCC) last February. Each Conlog is connected to its four neighbors by signal lines. These elements, which are programmed by special software, can either isolate defective chips or restrict use to those memory sectors known to be functional—unlike traditional techniques, where one defective memory bit necessitates rejection of the whole chip. Each 1-Mbit DRAM has been cut into 32 parts, each containing 32,000 bits—which means that, under normal operation, 80 percent of the available memory bits on the wafer are usable. For a 150-mm wafer integrating 202 1-Mbit chips, this would equal approximately 160 Mbits, corresponding to the claimed memory capacity of 20 MB. This means that, in mass production, the cost of this technology will be only 60 to 70 percent of that of a solid-state disk based on individual memory circuits.

Anamartic's originality lies in the interconnection program, which allows the definition of a continuous bidirectional data flow in the form of a spiral. The technology is conventional. The wafers are manufactured in Japan by Fujitsu in 1.3-µm complementary metal-oxide semiconductor (CMOS) technology. Fujitsu is also a shareholder in the British company and will market the Wafer Stack in Japan.

The wafers are protected by a layer of silicon nitride and are mounted on a printed circuit. Two wafers are mounted face to face to form a 40- MB module. An erasable programmable read-only memory (EPROM) flash memory mounted on the same substrate as the wafer loads the Conlog configuration program. It stores the addresses of defective chips or memory sectors and those of redundant memory sectors. This allows the configuration to be modified if initially functional memory sectors prove faulty, even if this occurs after a period of use. Anamartic's U.S. subsidary is responsible for both the product's marketing in the United States and the development of specific interfaces.



Every 1-Mbit DRAM is linked to a section of control logic (Conlog), which can isolate defective memory areas. Each Conlog is connected to its four immediate neighbors. Once programming begins, only the functional Conlogs are used.

DEFENSE INDUSTRIES

France, UK, FRG To Develop Radar System

90CW0158a Paris LE MONDE in French 23 Feb 90 p 9

[Text] France, the Federal Republic of Germany and the United Kingdom have signed an accord for the joint design of an anti-artillery radar. Christened Cobra, its main purpose is to locate enemy artillery cannons for regiments with multiple rocket launchers. Companies involved in the contract include Thomson CSF, Siemens and Thorn EMI Electronics in Europe and General Electric in the United States. The latter was chosen for its experience in the field and can open up the U.S. market to this European-produced system.

Development of the equipment, reckoned to cost over 1 billion French francs, should take 3 years, followed by a 2-year test period. It is estimated that mass production of the Cobra for the land forces of the three European countries will [bring in] over 4 billion francs. Other customer countries, such as Italy and the United States, are interested in the Cobra.

The system is a multi-function radar (with an active electron-scanning antenna using gallium arsenide) which is mounted on a vehicle. It rapidly and precisely locates enemy artillery cannons at distances ranging from 5 to 30 kilometers into the battlefield.

Rafale Able To Carry Nuclear Missile

90ES0656A Paris LE MONDE in French 16 Mar 90 p 14

[Article by Jacques Isnard: "Rafale Will Be Able To Carry Nuclear Missile"]

[Text] Toulouse—The Rafale will be able to carry a prestrategic ASMP (medium-range air-to-ground) missile. Chief Engineer Robert Finance, Rafale program director for the General Delegation for Armaments (DGA), made this disclosure on Wednesday 14 March at Toulouse, in remarks delivered to the regional French Aeronautics and Astronautics association (AAF), whose president is Engineer-General Jean-Claude Ripoll. It was the first time any official associated with the Rafale program—which is designed to produce a new combat aircraft for the French Navy and Air Force—has officially acknowledged this capability.

Noting that "this program was very thoroughly prepared" following a "series of very coordinated decisions," Mr. Finance detailed the kinds of weapons the Rafale could use in various missions. the Mica air-to-air missile (electromagnetic or infrared version), the Magic 2 and air tactical gun; Apache air-to-ground missiles that can be fired from a distance adequate to insure the pilot's safety; new-generation antiradar missiles or AS-30 laser missiles for ground attack missions; and AM-39 Exocet air-to-surface or supersonic anti-ship missiles (ANS) for combat against naval vessels.

The Rafale program director added that the aircraft could be armed with the ASMP missile, which carries a 300-kiloton nuclear warhead (15 times as powerful as the Hiroshima bomb) over a range of 100-300 km, depending on the altitude at which the device is triggered.

Thus the Rafale can be described as a "polyvalent weapons system," which will be able to handle the air defense missions of the Mirage 2000 C and Crusader, the ground attack missions of the Mirage 200 NP and Super-Etendard, and of course the prestrategic nuclear strike missions of the Mirage 2000 N and Super-Etendard armed with the ASMP missile.

"If all goes as scheduled," Mr. Finance opined, "the Rafale will be the first aircraft of the 1990's that integrates the new technologies." It will carry twice the weaponry of the Mirage 2000 and have about 35 percent greater range. Given these performance characteristics, the Rafale—if armed with a nuclear missile of greater range than the ASMP—should also be able to take over the Mirage IV's strategic mission, when the latter is retired from service in five more years.

But in his remarks to the audience in Toulouse, the program director did not discuss this possibility, which some in the General Staff are beginning to consider as a way of maintaining a "piloted" deterrent weapon.

The first prototype of the Rafale—five are planned in all—will have its initial flight sometime before 28 February 1991. The first production model will be the Rafale M adapted for deployment on aircraft carriers. At present it appears the Navy will require about 86 and the Air Force 250 of the aircraft.

Developments in Rafale Program Noted

Belgium May Participate

90CW0162A Paris LE MONDE in French 28 Feb 90 p 10

[Article by J.I.: "Belgian Industry Reportedly Joining Rafale Program"; first paragraph is editor's lead]

[Text] The Dassault group may soon announce an agreement to cooperate with Belgian industry on the Rafale program, while the competing project of the EFA European fighter aircraft suffers a year-long delay due to the British-German debate on the radar system.

A few weeks away from resumption of test flights of the Rafale demonstrator plane, equipped with the new SNECMA M-88 jet engine replacing the original American engine, the aircraft maker Dassault acknowledges great progress in drafting an agreement with Belgian industry. When the latter is complete, Belgian industry will reportedly participate in the development and mass

manufacturing of the Rafale, slated to equip the French air force and navy by the end of 1996 or beginning of 1997.

Discussions began in 1988. They were given the go-ahead by the French Defense minister, who traveled to Brussels for the occasion to debate the project with Belgian authorities having jurisdiction in the matter. At the time, a 10-percent participation by Belgian manufacturers was discussed. Depending on [the outcome of] contacts underway, today it seems that collaboration will remain well under 10 percent.

Proposals mainly concern the two companies SABCA and SONACA [extensions unknown]—for Rafale's airframe—who will finance 2 percent of the development of the last two prototypes and mass production. Under 1990 economic conditions, the development, industrialization and manufacture of 336 planes (250 for the air force and 86 for the navy) costs about 150 billion French francs, footed by the state and the manufacturers.

Next to Rafale, which may run into financial snags after 1993 if no foreign partner joins France, the rival airplane program, christened the European Fighter Aircraft (EFA), is currently experiencing some turbulence.

8,000 Jobs Threatened Across the Rhine

The British (a 33-percent share), West Germans (33 percent), Italians (21 percent) and Spanish (13 percent) are collaborating on this airplane project, whose cost for a total of 765 craft ordered is estimated at approximately 230 billion French francs by its promoters. The four European countries agreed to cooperate in November 1988. But their agreement covers only the development of the EFA and not its production, about which an understanding will have to be reached in 1991.

At the beginning of the year Great Britain and the Federal Republic of Germany put the kibosh on their quarrels, which had been dragging on for months, on the choice of radar: it is the British company Ferranti, recently rescued from bankruptcy, that will be in charge of it, but Bonn was given guarantees concerning any potential cost overruns. The upshot of these equivocations is that the first flight of the EFA, originally expected for 1991, will probably not take place before 1992, with the plane going into service after 1997.

Across the Rhine a controversy is brewing in political circles on the interest of maintaining or not such a costly program, now that disarmament in Europe and reunification of the two Germanys is around the corner.

The West-German defense minister remains a partisan of the project, despite admission that a newer, less expensive, version of the EFA should be built. The manufacturers, particularly Deutsche Aerospace, the aeronautics subsidiary of the Daimler-Benz group, are of the opinion that 8,000 jobs are on the line in the immediate term. But some Bundestag representatives are suggesting that the aid promised to the GDR be skimmed off the EFA's budget.

M-88 Engine Flight Tested

90CW0162B Paris LE MONDE in French 1 Mar 90 p 10

[Text] Equipped with an M-88 French jet engine to the left of its fuselage and an American F-404 jet engine to the right, the Rafale-A demonstrator plane made an initial 55-minute flight Tuesday 27 February from its Istres base (Bouches-du-Rhone). The plane, which is being used to develop the final version of the Rafale-D (D for discreet or "stealth"), has just undergone a long series of transformations in the workshops of the Dassault group.

In place of two General Electric F-404 jet engines that propel the demonstrator plane, the operational version of the fighter plane to be used by the air force and navy will be outfitted with two SNECMA [extension unknown] M-88 jet engines.

In its current test configuration, in which the M-88 will be tested in combination with the F-404 temporarily retained for reasons of flight safety, the Rafale-A reached an altitude of 40,000 feet (about 12,000 meters) and speed of Mach 1.4 (about 1,500 kilometers an hour). After a few other flights to check the compatibility of various on-board systems, the Rafale-A will be returned to SNECMA pilots. The latter will flight test the M-88, which has thrust of 7.5 metric tons (with post-combustion or supplementary afterburning).

FACTORY AUTOMATION, ROBOTICS

French Manufacturer Installs Advanced Robot System

90CW0158c Paris L'USINE NOUVELLE in French 1 Feb 90 p 57

[Article by S.F.: "Robot Arms That Understand Commands"; first paragraph is editor's lead]

[Text] Equipped with built-in electronics, intelligent robot arms can inspect or sort parts. One more step toward full automation of robot manipulations.

From simple mechanical fingers, robot pincers are evolving into true, intelligent peripheral devices. Able to perform part-inspection and -sorting tasks, they are widening the scope of robots in manufacturing handling operations.

The pincer position—open or closed—of a robot whose task is to move parts from one place to another must be known before it can be ordered to grasp. A sensor signals this position and sends the corresponding information: a closed pincer equals no part, an open one a part in hand.

The commonly-used method for determining pincer action is to program in dwell time: if, after a certain

amount of time, there is no signal indicating the presence of a part, the next sequence is engaged. The primary drawbacks of this method are a slowed rate of production (up to 40 to 50 movements a minute) and a lack of information on whether a part is actually there.

Intelligent robot arms—like those developed by New Mat, a principal French manufacturer (sales of 15 million French francs in 1989, 20 people)—use integrated electronics to memorize the positions of the pincer in relation to the part. The system combines a sensor, which measures the movement of the piston driving the pincer, and a microcontroller linked to the programmable automaton that runs the robot.

What these robot arms actually do is set up a dialog between the automaton and the pincer. By telling the robot its position relative to the part, the pincer acts as a monitor, and can intervene in the manufacturing process in new ways. Faulty positioning of parts can be detected. If the latter arrive, for instance, facing the wrong way, they will be repositioned during transfer instead of rejected. In simple applications, a video-monitoring system can be dispensed with. Other advantages: the robot arms can sort out defective parts in vibratory hopper feeders, or select, in order, components of the desired size for assembly.

In the opinion of Philippe Roudaut, manager of New Mat, intelligent robot arms are destined to replace current ones. The Sannois firm will begin marketing them during the first quarter. Other robot pincer manufacturers—the German company Schunk and the French firm CCMOP—are also going this route.

LASERS, SENSORS, OPTICS

France Adopts Three-Year Industrial Laser Program

90CW0139 Paris L'USINE NOUVELLE in French 25 Jan 90 p 22

[Article by Stephane Farhi: "A Boost for Industrial Laser; The Ministry of Industry Frees Fr20 Million"]

[Text] **A program associating suppliers and users was just launched to promote industrial laser applications.**

Seven industrial laser application projects associating source manufacturers, system and machine designers and users have just been included in the industrial laser program. Financed two-thirds by businesses and one-third by the Ministry of Industry, the 3-year Fr60-million program aims to pull the supply by the demand by bringing users and suppliers together. According to a 1988 study made by M2I for the Ministry of Industry, the French production of industrial laser systems is not one-tenth that of the FRG (less than Fr200 million compared with over Fr2 billion). And laser penetration in the industrial fabric is smaller by one half in France: 3.5 percent of French businesses employing over 100 people own a laser, compared with 7.3 percent in the FRG.

Rather than undertaking a costly and chancy sectorial plan (remember the machine-tool plan, the components plans), the Ministry of Industry chose to be practical and open-minded. The program regroups practically all French manufacturers of industrial lasers: Adron Sources (a subsidiary of Lectra Systems, created in 1988), Quantel (now part of Unilaser which is controlled by Aerospatiale), BMI and Sopra (the only French manufacturer of excimer lasers); and also robot manufacturers such as Renault Automation, Eurosoft Robotics and Micro Control, and large companies: Thomson, Aerospatiale, Essilor.

Since Cilas [Industrial Laser Company] (the former CGE [General Electricity Company] subsidiary now owned by Aerospatiale) has given up its industrial laser activities, France no longer has a general laser-source manufacturer of adequate size. It also lacks a major outlet, such as the powerful machine-tool industries of Germany and Japan. Trumpf, the leading German manufacturer of CO_2 lasers with Rofin Sinar (240 lasers in 1989), is also the leading manufacturer of sheetmetal cutting machines, which absorb 70 percent of its laser production. This enables Trumpf to produce 160 laser-cutting machines per year, 10 times as many as the French company Limoges Precision.

The chance of French manufacturers may reside in the dynamism of the demand. According to M2I, France still represents only 2.5 percent of a world market estimated at $700 million (Fr4.2 billion), but the average French annual growth rate for 1988-1991 is estimated at 18 percent (15 percent for the FRG, 16 percent for Europe). According to the Power Laser Club, about 450 laser systems (CO_2 and YAG [yttrium-aluminum garnet]) are now in operation in France. Laser dissemination in the industry—in particular in small to mid-size businesses—could also rely on a regional network of about 10 technology transfer centers.

The drawback of this organization is a certain scattering of efforts. Therefore, both the ministries involved (Industry and Research) and trade organizations are now considering the advisability of creating a Laser Technology Institute, similar to the German Fraunhof Laser Technology Institute of Aachen which employs 200 researchers. This creation would be a tangible manifestation of a will to be represented in a strategic sector which requires considerable research and development resources.

Pulling the Supply by the Demand

Seven industrial laser projects were adopted:
- Automation of a surface-treatment machine using a YAG laser; partners: Adron Sources and Ateca.
- Electric cable marking system; Aerospatiale.
- Brazing of components on electronic cards with a CO_2 laser; Eurosoft Robotics and Quantel.

- Marking machine using a YAG laser; Micro Control.
- Cutting robot with multiple articulations, using a YAG laser and optic fiber; Renault Automation.
- Identification marking with an excimer laser; Sopra and Essilor.
- Microwelding of optoelectronic components using a YAG laser; Thomson Hybrids and BMI.

Four of these seven projects deal with specific applications. This illustrates the "niche" strategy adopted by French businesses.

MICROELECTRONICS

EC Council, Commission Approve Japanese DRAM Deal

Council Approval

90AN0155 Brussels EUROPE in English 19 Jan 90 pp 7-9

[Report: "EC Council Accepts Arrangements Concerning Price Undertakings Offered by Japanese Exporters of DRAM Semiconductors—Commission Is Now in Position To Formally Adopt Regulation"]

[Text] The long procedure aimed at implementing the arrangements concluded with the Japanese producers of DRAM (Dynamic Random Access Memory) semiconductors has reached the penultimate stage. The Community Council decided not "to adopt a ruling different" from that of the Commission.

Consequently, the latter may from the end of this week formally adopt the regulation which approves the price undertakings offered by Japanese exporters. This regulation will be published in the OFFICIAL JOURNAL OF THE EUROPEAN COMMUNITIES in the middle of next week and will immediately enter into force.

EUROPE recalls that this case originated in February 1987, when the Commission received a complaint lodged by European manufacturers of electronic components on behalf of Motorola (UK), Siemens (FRG), SGS Microelettronica (Italy), and Thomson (France), reporting dumping practices by Japanese exporters and injury for Community industry. The case was quite sensitive, since the Commission had to take account simultaneously of the interests of Community DRAM manufacturers and those of the user industry, which is quite diversified and wants to obtain semiconductors at the best possible prices. Imports originating in Japan are of fundamental importance for this industry, since they account for 70 to 80 percent of Community needs. Moreover, Japanese manufacturers argued that the four European companies mentioned above do not account for Community production as a whole; according to them, IBM should also be considered a Community producer (the company manufactures and assembles DRAMs in a plant located near Stuttgart), and Philips should be considered a potential producer. However, neither IBM, Philips, nor companies assembling DRAMs in the Community were included among the plaintiffs.

To these economic issues were added very complex technical questions for the determination of the normal value of DRAMs. The reasonable profit margin and export prices, for the taking into account of R&D expenses (fundamental in this area), for comparisons between the various types of DRAMs, etc. The Commission noted a major decrease in the price of DRAMs during the period covered by the investigation, and reached the conclusion that these prices were generally at levels below production costs. There was later a certain price increase (after the period covered by the investigation), but the investments of the Community companies concerned were not profitable for a certain period and led to considerable financial losses.

One additional element intervened during the investigation: the agreement concluded between Japan and the United States, which led the Japanese Government to practically force its exporters to increase sales prices on the European market.

In the final analysis, the Commission came to the conclusion that the best solution, which takes account of all interests at stake, resides in price undertakings by the Japanese exporters. The latter accepted the principle; long negotiations were then required to draft the criteria and the content of these undertakings. Last July, these negotiations were concluded and the Commission was able to finalise its draft regulation in August. It was a Commission regulation (rather than a proposal to the Council), since the Commission alone is competent to accept price undertakings, provided it consults the Member States. In the fall, the Commission undertook this consultation and one Member State, Ireland, opposed the draft regulation. The Commission was thus obliged to refer the matter to the Council. After last-minute changes in the text, the Commission's draft regulation was forwarded to the Council on 18 December 1989; it had one month to rule differently, if it considered it desirable.

During the debates held within the Council, it appeared that eleven Member States were in favour of the solution selected by the Commission, while Ireland confirmed its opposition. The only precaution required of the Commission is that it regularly informs the Member States about the evolution of the situation and its possible initiatives. Consequently, the Council practically approved the Commission's move, accompanied by two declarations:

1) Declaration of the European Commission: If the Commission is informed by the Member States that the price undertaking offered by Japanese exporters results in anomalies on the Community DRAM market, the Commission will rapidly review the situation and take

the necessary steps, notably consultations with the Japanese manufacturers/exporters. The Commission will inform the Member States about the action it has taken.

The Commission is aware of the fact that the expiration of the agreement on semiconductors concluded between the United States and Japan might also result in major repercussions for the Community DRAM market. Therefore, the Commission is ready to undertake a review of the measures adopted if the American measures concerning DRAMs originating in Japan are effectively and definitively abrogated in September 1991.

The Commission is also prepared to periodically inform the Member States, within the framework of the antidumping Committee, of developments in the Community market for DRAMs.

2) Statement by Ireland. The Irish delegation is against the solution chosen, because it will be damaging to both Irish and EC interests. It particularly finds that it is unfair to extend the price commitment to new DRAM products, because no unfair trading in respect of these products has been alleged. It is likely to disadvantage EC industry users by increasing their costs and ultimately disadvantage all consumers. Ireland also finds that the contested measure leaves the Community open to accusations of protectionism and reinforces the cartellisation of markets in DRAMs.

The arguments made in the Irish statement were taken into consideration by the Commission, but it found that it is vital for the EC to have viable semiconductor production and that the DRAM technology is a fundamental basic technology. Without European production of DRAM, the European computer industry would depend entirely on third countries which could impose their models and their prices. The Commission is contesting the thesis that the European industry overall would be harmed by the application of the arrangement and underscores that it has made appropriate provisions so that industries using DRAM products will be able to obtain them at competitive prices.

The technical content of the measures decided by the Commission (antidumping duty of 60 percent, which would remain theoretical because it would not be applied to Japanese manufacturers who have made price commitments; minimum prices set at the level of production costs plus 9.5 percent) was anticipated in EUROPE on 5 December.

Commission Approval

90AN0155 Brussels EUROPE in English 24 Jan 90 p 7

[Report: "EEC-Japan: European Commission Has Approved Arrangement With Japanese Producers of DRAM Semiconductors Setting Up Minimum Prices (Including for New Products)"]

[Text] The European Commission today adopted the regulation accepting price undertakings offered by Japanese DRAM (dynamic random access memories) semiconductor exporters. This regulation will be published in the OFFICIAL JOURNAL OF THE EUROPEAN COMMUNITIES on 25 January and will immediately enter into force. This event marks the solution to an anti-dumping proceeding initiated in 1987 and which occupied Community institutions and economic milieux for a long time. The effect of the regulation will be twofold:

- to guarantee that Japanese DRAM's will no longer be exported to the Community at dumping prices;
- to guarantee at the same time that the minimum prices will not be too high, so as to prevent extra expense for user industries; these minimum prices must correspond to costs plus a modest profit margin (9.5 percent).

The European Commission finds that this regulation preserves the interests of Community DRAM manufacturers (the complaint was lodged by the EECA [European Electronic Component Manufacturers Association] on behalf of Siemens, Thomson, SGS, and Motorola) as well as those of user industries. It must be borne in mind that in 1987 the Japanese held 70 percent of the European DRAM market, compared to 7.1 percent held by Community producers (and 9.7 percent by South Korea, 6.2 percent by the United States, and 6.5 percent by other Southeast Asian countries).

The Japanese firms that have ordered price undertakings are: Fujitsu, Hitachi, Matsushita, Mitsubishi, NEC, NMB, OKI, Sanyo, Sharp, Texas Instruments Japan, and Toshiba. The commitments cover not only DRAM's currently being produced, but also the more powerful new-generation models that are being researched.

The European Commission will reexamine the situation at the end of 1991, if the agreement between the United States and Japan on semiconductors expires, as is currently planned. In addition, the Commission will constantly survey the European DRAM market to intervene if need be.

CNET Demonstrates HDMAC Circuit Modifications

90AN0158 Paris FRENCH TECHNOLOGY SURVEY in English Dec 89 p 9

[Article: "Writing Connections Directly Into an Integrated Circuit"]

[Text] The [French] National Telecommunications Research Centre (CNET) recently demonstrated how a function could be modified in a particular microchip already forming part of a circuit. This new technique has an economic advantage in enabling the circuit development time to be reduced.

The modifications may be made by direct inscription. The circuit is placed in an enclosure containing a gas selected according to the required modification. A high-power laser beam is focussed on the surface of the circuit and induces a controlled local increase in temperature. The gas decomposes, leaving on the circuit surface a deposited metal spot 1-2 micrometers in diameter. By physically moving the circuit, a line is drawn to join two points in the circuit.

The first circuit modification was carried out last July on an early version of a digital/analogue converter (DAC) for HDMAC signals, built using the CNET CMOS 1T production line. A connection had to be made between an input terminal and a tungsten line 1.2 micrometres wide and covered by a layer of insulation. The insulation was opened by selective thermal engraving in the presence of tungsten hexafluoride and the connection made to the outside by means of nickel line. This modification made it possible electrically to check the circuit and to demonstrate a hidden fault, the immediate correction of which reduced the assembly time of the circuit in which this DAC is incorporated.

NUCLEAR ENGINEERING

Italy: Newly Developed Superconducting Magnet Described

90MI0091 Rome FINMECCANICA NOTIZIE in Italian 31 Oct 89 pp 16-17

[Text] The Milan-based LASA (Laboratory for Applied Superconductivity and Accelerators) has developed a superconductor electromagnet for a heavy ion accelerator that is the first of its kind in Europe. Ansaldo ABB Components participated in the project under the scientific supervision of the INFN (National Institute for Nuclear Physics). The company had previously taken part in the construction of the HERA [Electron-Proton Collider Ring] in Hamburg.

In a particle accelerator the magnet's function is to force the particles to move along a spiral trajectory from the source to the target. The magnet, including iron and coil weighs 200 metric tons and is four meters in diameter and three meters long. The material used for the cables is a titanium and niobium alloy, a traditional type of superconductor material which functions at about 270 degrees below zero when the alloy loses its electrical resistance completely. The use of a superconductor material results in the creation of very intense magnetic fields of up to 6 Tesla. Another advantage is the magnet's reduced size with respect to traditional magnets. This reduction in size is also accompanied by a considerable reduction in costs.

SCIENCE & TECHNOLOGY POLICY

Italy: National Bioelectronic Research Program Outlined

90MI0090 Milan ITALIA OGGI in Italian 5 Dec 89 p 41

[Article by Michela Fontana: "The Italian Road to Computer Science Via the 'Biochip'"]

[Text] The deadline for the presentation of proposals for projects under the National Research Program on Bioelectronic Technology, launched last September by the Ministry for the University and Scientific and Technological Research, will expire on 22 December. Over the first months of 1990, the companies or consortia that have been selected will sign the first contracts with research centers and universities.

The program has received approximately 100 billion lire in funding for the first three years (10 of which are reserved for training), and is "directed toward the development of highly innovative technologies and strategies with medium-term industrial applications." It is the first program in Italy whose goal is to develop molecular electronics, a field of study that combines electronics, biology, chemistry, and computer science and that is gaining a foothold in the world's most advanced industrial and university laboratories. This field is destined to have applications in many industrial sectors and its ultimate research goal is the innovative objective of constructing devices to process information based on the use of biological substances, the so called "biochips." This term refers to plates like those used in today's chips but constructed with biological material, such as proteins, instead of silicon. According to researchers, proteins which carry out vital functions in the human body should be able to perform information processing functions that are much more sophisticated than those now carried out by electronic circuits. For example, this would permit the construction of computers which are more compact, flexible, and intelligent than those currently in use.

"The biochip could be the final result of well-defined research," Claudio Nicolini, professor of biophysics at the University of Genoa and the principal promoter and inspirer of the national program, recently explained.

According to Nicolini, two areas of research must be developed to construct chips with biological material. These areas include protein engineering and neuron microelectronics, both of which are already of great strategic importance.

The first area aims at the construction of proteins not found in nature by using genetic engineering methods. These proteins can be utilized in the chemical, food, and agricultural industries and subsequently the electronics industry. The second area, neuron microelectronics, is

concerned with the production of "neuron" chips whose architecture is based on the organization of the nerve cells inside the brain.

In the ministerial program these sectors are combined with first generation bioelectronics, which involves developing biosensors, devices halfway between electronics and biology that can be applied in medicine and environmental conservation. They are used, in fact, to identify and measure organic and biological substances found in the human body and the environment. "We are satisfied with how the program was launched," stated Giuseppe Mondelli, president of CIREF, a consortium of companies that includes SGS-Thomson, Montedison, Elsag, Sorin, the Donegani Institute, and Automa, and was created two years ago precisely to promote studies on the biochip. Mondelli explained that "even if the program is risky given its highly innovative nature, our country should have an opportunity to become competitive at the international level."

Carlo Rizzuto, director of the Interuniversity Consortium for the Structure of Materials, added: "The projects presented are numerous and varied. It is a matter of seeing where success can be achieved. It is nevertheless very important that the program has stimulated a great interest among the most active research groups in our country. We also hope to be able to attract the highly qualified Italian scientists who now conduct this research abroad back to our laboratories."

Government To Submit Microelectronics Plan

90AN0137 Amsterdam COMPUTABLE in Dutch
15 Dec 89 p 17

[Excerpts] The Hague—Within the next few months, Minister of Economic Affairs Andriessen will present a policy plan on microelectronics aimed at establishing a framework for the stimulation of microelectronics activities in the Netherlands over the coming years. The plan must encourage industry to implement even more advanced forms of microelectronics and will presuppose that closer association must be sought with European developments in this field. The aim is to enable Dutch trade and industry to profit as much as possible from future results of the EUREKA project for the joint development of IC technology, the Joint European Submicron Silicon Initiative (JESSI). [passage omitted]

Andriessen also announced that Dutch universities are taking an active part in the JESSI program. The Innovation-Oriented Research Program for Integrated Circuit Technology (IOP-IC) clearly contributed to the initial stages of JESSI. Since then, many Dutch universities have been involved in project proposals which have been submitted to the JESSI board. In addition, the Society of Microelectronics Centers (SCME) will be linked to the Innovation Centers network as of the beginning of next year. This means that SCME will be included in the same administrative and financial structure as that of the Innovation Centers. Thereafter, it will be gradually integrated further in the Innovation Center network.

Following last week's announcement that the project for the development of Philips 4-Megabit static random-access memory (SRAM) had gained official JESSI status, it now appears that a project has also been approved which involve the establishment of a "joint framework" for computer-aided design (CAD) applications. The aim is to create a joint European basis for the development of CAD programs. This will enlarge the similarities between and compatibility of CAD programs and make CAD programs more easily interchangeable. Program elements will be more widely usable, allowing faster and better operations. [passage omitted]

Netherlands: Funding for Neural Network R&D Program

90AN0139 Rijswijk PT/AKTUEEL in Dutch
29 Nov 89 p 1

[Article: "SPIN Project Closes With Neural Network Research Program"]

[Excerpts] The Information Science Stimulation Project (SPIN) team has allocated 3.5 million Dutch guilders to a program for neural network research. The overall cost of the program, which will run for 4 years, amounts to 9.6 million guilders. [passage omitted]

Institutes

The neural network research is being conducted by several institutes, including the Catholic University of Nijmegen, the Institute for Applied Scientific Research (TNO), the University of Amsterdam, and the State University of Leiden. The following seven companies are sponsoring the project: Shell, Hewlett Packard, Digital Equipment, Arcobel, Volmac, BSO, and Philips.

This is the 10th and last program conducted within the framework of SPIN. During the 4 years of its existence, SPIN has spent as much as 75 million guilders to stimulate research in the field of information science. The SPIN project will come to a close on 1 January 1990, but its activities will be continued by StiPT, the Ministry of Economic Affairs' Office for Technological Policy Implementation.

COMPUTERS

CAD Software for GDR's K-1845 Computer Described

90CW0129a East Berlin RECHENTECHNIK-DATENVERARBEITUNG in German
No 1, Jan 90 pp 5-7

[Article by Dr. Jochen Winkler, VEB Robotron-Elektronik Dresden]

[Text] The K-1845 computer and its variety of peripheral equipment enables the user to format complicated and efficient CAD/CAM application solutions, the effective development of which can be achieved with the following basic graphic and geometric software:

—GKS1800 (2D) /1/ Implementation of the Graphic Core System (GKS) corresponding to ISO 7942 and TGL 44610;—GKS1800 (3D) Implementation of the Graphic Core System for Three Dimensions (GKS-3D) corresponding to ISO 8805 and TGL 44611 /2/;—GEKO1800 /2/ Geometric modeling software (border and CSG display) in polyhedron approximation;—GEMO1800 /3/ Geometric modeling system for linear and circular geometry; and—GBS1800 Complex CAD basic system for 3D mechanical construction.

The GKS1800 continues the trend in the GDR to provide the application programmer with a uniform, internationally standard graphic interface in all Robotron-produced computers. In addition, graphic data can be exchanged between various systems using the GKS1800 image data set. Various complex geometric modeling tools were developed using GEKO, GEMO, and GBS1800 /4/. The most comprehensive system is GBS1800. It supports modeling, storage, processing, visualization, drawing preparation, and piece list generation of complicated 3D geometric objects in volume presentation. The following is an overview of the aforementioned software.

GKS1800 (2D)

The Graphic Core System (GKS) has been the international standard since 1985 for defining the graphic interface between an application program and a graphic system.

GKS1800 is a standardized implementation on the RVS K-1840/K-1845 computers with the SVP1800 or MUTOS1800 /5/ operating systems. FORTRAN-77 /6/ was selected as the language shell. The following devices are currently integrated into GKS1800:

—Intelligent Graphic Terminal IGT K-8918;—Intelligent Graphic Terminal IGT K-8919;—A2 Plotter PLT K-6411;—A0 Digitizer DG K-6404/20/30;—Matrix Printer ND K-6313/14;—A0 Plotter DGF 1208 3.5G; and—selected imported devices.

Although the integration of additional devices is being planned, the user can also choose to add on devices himself.

GKS1800 achieves the maximum GKS performance level, level 2c. A variant at level 0a is also available for applications with few passive requirements.

In addition to the functions defined in the GKS-Standard, the GKS1800 contains numerous options for generating display elements. These include:

—22 type fonts (including Cyrillic);—128 seriph types;—circular arcs, sectors, or segments (filled in selectively);—elliptical arcs, sectors, or segments (filled in selectively);—disjoint polyline;—polygon (filled in selectively); and—rectangle (filled in selectively).

The GKS1800 image data set corresponds to the E add-on of the GKS-Standard /7/. Two codes (ASCII, RVS internal code) are possible. Data transfers, which were already produced with GKS1600 or DIG1600 /5,8/ are also possible for GKS image data sets.

GKS1800 is the result of close cooperation between Wilhelm-Pieck University Rostock and Robotron Dresden.

GKS1800 (3D)

Three-dimensional functionality is becoming increasingly necessary for many application solutions. Because GKS-2D has only limited applicability here, this task has been accomplished by the GKS-3D since 1988. Upward compatibility to the GKS-Standard is guaranteed by the fact that GKS-2D is a subset of GKS-3D. Every application program with a GKS-2D interface can immediately be run on GKS-3D implementations. Considerable expansions of the GKS-3D over the GKS-2D are:

—3D display elements;—fill field sequence (display element with border attributes);—3D system and transformation of coordinates including projection transformations; and—ability to connect with processes for removing hidden surfaces and edges (HLHSR).

GKS-3D is essentially a 3D system. Although it also contains 2D primitives for running application programs with a GKS connection, these are immediately converted into 3D display elements. In this way it is also possible to describe a planar object and subsequently manipulate it in a 3D space.

The following display elements are stipulated:

—continuous line (sequence of 3D points that are extended to interconnect;—polymarks (sequence of 3D points, each with an allocated centered symbol);—text (character sequence at a defined position in a defined plane within the 3D space);—fill field (planar polygonal surface (hollow, colored, patterned, or hatched) on a defined plane within the 3D space);—fill field sequence (number of polygonal surfaces within a

plane of the 3D space, which are processed together, with alternative display of the borders);—cell matrix (made from a parallelogram composed of single-sized and monochrome cells on a defined plane within the 3D space); and—generalized display element (VDEL) for using specific device intelligence for such things as circular or elliptical arcs.

The visibility of edges can be controlled using the fill field sequence display element. A fill field sequence can contain gaps; it also may not be continuous.

The number of attributes for the display elements was expanded compared with GKS-2D. GKS-3D contains, for example, not only border attributes, but also the new attributes HLHSR-flagging, HLSR-mode, and projection-index, which are allocated to every output primitive. HLHSR-flagging is used to create classes for HLHSR processing.

Depending on the work station, the HLHSR-mode attribute controls the selection of appropriate processes to solve the problem of hidden edges and surfaces. Depending on the work area, the projection-index describes the standpoint and line of sight of the observer, as well as the type of projection (e.g. parallel, perspective), and the clip volume of the 3D scene.

GKS-3D contains five 3D coordinate systems:

—world coordinate system;—standardized coordinate system;—projection coordinate system;—standardized projection coordinate system; and—device coordinate system.

Transition between the coordinate systems is accomplished with the following transformations:

1. The standardizing transformations are used in composing various partial images, which are described in their own (world) coordinate system in a common standardized coordinate system.

2. The segment transformation is an image within the *Standardized Coordinate System*, whereby defined images (segments) can be inserted in accordance with the desired size and the arrangement of the partial images to one another.

3. The standpoint and line of sight of the observer of the 3D scene is determined by the projection coordinate system. The projection orientation transformation is implemented with every point of the graphic display elements using matrix multiplication. GKS-3D contains help functions for producing the necessary 4 x 4 transformation matrix. The projection orientation transformation is followed by the projection image transformation, which supports the parallel or perspective projections. This transformation is also implemented using homogeneous coordinates by means of a 4 x 4 matrix and a 3D projection window.

4. The device transformations are images of the 3D standardized projection coordinate system in the respective specific 3D device coordinate system. Because the graphic output devices allow only two-dimensional displays, the z-coordinate is disregarded after being used selectively in the HLHSR-processing.

GKS-3D supports the same input classes and modes as GKS-2D (locator, line giver, value giver, selector, picker, text giver). The difference lies in the 3D functionality. Analogous to the output pipeline, all inverse transformations are also images between 3D coordinate systems. The projection index and the standardizing transformation number characterize the inverse transformations. The results correspond to those of the GKS-2D, except for the input classes of locator and line giver. If there is no 3D input device available (e.g. 3D digitizer), the z-coordinate can also be input via the keyboard or the value giver. GKS1800 (3D) is a standardized implementation /9/. It is completely upward compatible to the GKS1800 (2D). GKS1800 (3D) is available for the SVP1800 and in 1990 will be available for the MUTOS1800 as well. The GKS1800 (3D) was developed jointly by Robotron-Elektronik Dresden and Wilhelm-Pieck University Rostock.

GEKO1800

The modeling system GEKO1800 is a basic software for modeling 3D geometric objects in border and CSG displays. It has a special purpose language for defining, storing, modifying, and graphically displaying geometric objects /2,10/. GEKO1800 consists of three building blocks: the language portion, the geometry portion, and the output portion for passive graphic display. The GKS1800 is the graphic interface, and the operating system is SVP1800.

GEKO1800 is a 3D modeler for bodies with flat surfaces and borders. Set operations (union, average, difference) are defined on these objects.

The output portion contains sight and projection transformations, i.e. the standpoint and line of sight of the observer of the 3D scene can be selected as desired. Some views are already predefined (horizontal and vertical projection, side elevation, orthogonal projection, orthogonal axonometry (isometry, dimetry), cavalier projection). Hidden edges can be extracted.

In addition to the operations for defining and modifying geometric objects, rotation and translation operations are also possible.

One can work off GEKO1800 both in conversational and batch processing. It was developed by the Technical University Dresden.

GEMO1800

The GEMO1800 subprogram package is used to model, calculate, and construct geometric objects in a 3D space. It consists of three components:

—GEMO-G (modules for unit operations);—GEMO-P (modules for set-theoretical operations with polyhedrons); and—GEMO-R (modules for rotation objects).

With the GEMO-G subprogram, calculations can be made between geometric objects (e.g. parallelism, section formation, distance calculation) and constructions (e.g. of verticals and tangents).

With the GEMO-P subprograms one can model any kind of flat-surfaced, bordered geometric objects by means of modified set operations on elementary polyhedrons (e.g. parallelepipedons, prisms) and the bodies resulting from them. The description of the objects occurs in border representation.

With the GEMO-R subprograms one can model surfaces or bodies of rotation, which are composed of cone, cylinder, or torus portions. GEMO1800 includes the following geometric objects in the modeling:

—point;—curve (straight, segment, progression, circle, circular arc);—surface (polygonal surface, contoured surface, circular area, gliding plane, surface of rotation—including cylinder, cone, and torus surface—polyhedral surface); and—bodies (polyhedron, sphere, gliding planes, body of rotation—including cylinder, truncated cone, torus).

The available operations include:

—relationships test (incidence, parallelism, orthogonality);—metric unit operations (e.g. distance determination, angle calculation);—geometric unit operations (connecting, cutting, constructing parallels, verticals, and tangents);—transformations (translation, rotation, scaling, reflection); and—modified set operations (union, average, difference).

GEMO1800 does not contain any display routines.

The user receives the GEMO subprograms in the form of an object module library. They are written in FORTRAN-77, and the operating system is SVP1800. Its geometry interface is the IGOO Interface /11/. As a basic software, the GEMO1800 can be used to rationally develop CAD user software. It was developed by the Technical University Dresden.

GBS1800

The geometric modular system GBS1800 is a CAD system, whose high efficiency makes it suitable for solving challenging tasks in the construction of spatial mechanical parts and componentry. It can be used in machine construction, automobile manufacture, equipment and plant engineering, in light industry and civil engineering. The GBS1800's integrated data bank system can store geometric, technical, and technological data. GBS1800 possesses numerous functions for modeling, visualization, dimensioning, drawing preparation, calculation, data management, piece list generation, provision of NC data, and product data exchange (IGES Interface) of technical 3D objects.

GBS1800 can be used immediately as a turnkey interactive system. Dialog is supported by menu and window technology as well as by extensive information and help services.

GBS1800 can be connected directly to its own application solutions via its language interface. Because of the availability of all internal GBS routines, the language is highly functional, understands FORTRAN instructions, and runs via the internal data structure.

The functions of the GBS1800 are particularly numerous in its capacity as a volume-oriented CAD system for the modeling of geometric objects (CSG and border representations). In addition to the exact analytical description of the objects, there is a polyhedral convergence of the object surface in the data base, particularly for the support of graphic interaction.

The GBS1800 integrates the following object classes:

—points;—curves (progression, circular arcs, BEZIER curves, contours, bezels, roundings, construction subsidiary lines);—surfaces (closed curves, flat surfaces, polyhedral surfaces, BEZIER surfaces, rotation and translation surfaces);—bodies (prisms, cylinders, cones, bodies of rotation and translation, tubes, enveloping volumes with free-form surface bordering); and—drawings (combination of objects, e.g. componentry).

Creating parameters for geometric objects is also possible, such as performing set operations (union, average, difference).

The construction of mechanical piece parts is supported by many construction aids, whereby construction elements such as planes, vectors, axes, centers, lengths, factors, radii, and angles are used. Auxiliary construc tions (e.g. medians, mean perpendiculars, verticals, normal lines, projections, and intersecting points) are also suited for this.

GBS1800 provides an efficient visualization of geometric objects, including:

—definition of up to 10 light sources and 16 projections simultaneously;—any standpoint and line of sight;—parallel or perspective projections, including the use of predefined projections (e.g. horizontal, side, and vertical projection, axonometric projections, central projections, panoramic projections, fisheyes);—selective extraction of hidden edges with lattice-sided display;—colored, tinted display of bodies using Gouraud tinging;—variable partitioning of the screen to display several projections simultaneously;—interactive work in every projection through inverse visual transformation; and—zoom and pan functions.

A CAD-system for mechanical construction would be incomplete if it did not also contain user-friendly functions for dimensioning and drawing preparation. The following functions are available for dimensioning:

—semiautomatic dimensioning with direct transfer of the dimension drawings from the object data base;—different measurement methods (circular, line, diameter, radius, and angle dimensioning);—text and symbol generators;—specification of tolerances and roughnesses;—ability to edit the dimensioning, including standard values and symbol tables;—creation of one's own and modification of already existing character sets; and—large number of graphic attributes (e.g. line width, line type, seriph, text justification) for displaying dimensioned drawings.

The further usage of dimensioned objects to make complete construction drawings is also supported. In this way, drawing frames and title blocks can be defined and dimensioned objects can be positioned on the drawing as desired. Drawings can be stored separately, changed later, or transferred into a plot data set for output.

To support the design engineer, there are calculation functions to determine geometric (point coordinates, distances, angle, circumstance) and integral characteristics of objects (curve length, surface contents, volume, mass, center of gravity, moment of inertia). A collision test is also possible.

GBS1800 contains its own data management system for temporary and long-term storage of technical 3D objects and drawings. This includes depositing data in various hierarchically arranged data bases, which belong to a certain subproject or to an overriding project. Objects of general interest (e.g. standard tables, dimensioning tables, character sets, symbol tables) are stored in specific data bases. GBS1800 provides the definition of access rights for reading and writing on the specific data bases, so that a high degree of data security is achieved. The principle of referencing subobjects is applied in the data bases in order to avoid multiple storage.

The following modules are available for communicating with other systems:

—module for connecting with the VDA-FS surface interface;—module for connecting with the EGES 2.0 interface for product data exchange; and—module for transferring standard parts from a standard parts library.

A module for connection with the FEM is under development. Also planned are an expanded free-form surface module and modules for realizing NC-interfaces for boring, rotating, and 2.5-axis milling as well as 3- and 5-axis milling of free-form surfaces.

The technical device prerequisites are the RVS K-1840 or K-1845 computers (at least 8 MByte general memory and 70 MByte external memory) with the SVP1800 operating system. The graphic Display IGT K-8919 (19" color monitor) and/or the EC-1834 and A-7150 personal computers with appropriate coupling software are used for graphic interaction. In addition, plotters produced by Robotron and suitable imported devices were integrated. The GBS1800 geometric modular system was a joint effort by Robotron-Elektronik Dresden, the Central Institute for Cybernetics and Information Processes, the GDR Academy of Sciences' Institute for Data Processing and Computer Technology, and Wilhelm-Pieck University. It is currently being upgraded with additional expansion levels.

All the aforementioned software packages can be obtained from Robotron Berlin/Magdeburg factory.

Footnotes

1. Multiple authors: Graphic Core System (2D/3D), version 2.0 and 3.0 GKS1800—application description 6/88. Programming description:—information (version 1.0) 6/88—instructions for the systems analyst (version 1.0) 6/88—instructions for the programmer (version 1.0) 6/88—output advice

2. Multiple authors: geometric construction (3D modeler, version 1.0 GEKO188—application description 11/87, programming description 11/87

3. Multiple authors: GEMO1800 geometric modeling system—application description 9/88, programming description—instructions for the programmer 9/88

4. Multiple authors: GBS1800 basic system, application description 9/89, system handbook 9/89, user handbook 5/89 (developmental version)

5. Mikut, M.; Urban, B.: Graphic core system GKS1800 NTB 32 (1988) 3 pp. 90-93

6. ISO 8651 Information Processing Systems-Computer Graphics, Graphical Kernel System (GKS), Language Bindings Part 1: FORTRAN Part 2: PASCAL Part 3: ADA Part 4: C

7. ISO 7942 Information Processing Systems-Computer Graphics, Graphical Kernel System (GKS), Functional Description 1985

8. Baier, W,; Mikut, M.: The image data set of the GKS1800 NTB 32 (1988) 4, pp. 103-107

9. ISO 8805 Information Processing Systems-Computer Graphics, Graphical Kernel System for Three Dimensions (GKS-3D), International Standard Oct. 1988 10. Hartwig, A.; Mager, K.: 3D Modeling with GEKO, research texts, computer geometry (documentation), publication series WBZ/IV of the Technical University Dresden 86/86 11. Ludwig, Ml; Richter, Ch.; Klix, W.D.: Interface for geometric objects and operations (IGOO), Preprint Technical University Dresden, 1985, No. 07-05.85 12. ISO 8806 Information Processing Systems-Computer Graphics, Graphical Kernel System for Three Dimensions (GKS-3D), Language Bindings Part 1: FORTRAN Part 2: PASCAL Part 3: ADA Part 4: C 13. TGL

44510/01 Graphic Core System (GKS), 2D Graphics Language Links, FORTRAN part 14. TGL 44530/13 Information Processing Terms and Definitions for Computer Graphics (ISO 2382) 15. TGL 44610 Graphic Core System (GKS), 2D Graphics 16. TGL 44611 Graphic Core System for Three Dimensions (GKS-3D)

LAN Software for GDR's EC-1834 Computer Described

90CW0130a East Berlin RECHENTECHNIK-DATENVERARBEITUNG in German
No 1, Jan 90 pp 7-10

[Article by Holger Schleife and Michael Philipp, VEB Robotron-Karl-Marx-Stadt Accounting Machine Factory]

[Text] The current status of local nets for the 8- and 16-Bit PCs offered by Robotron is as follows:—A series of publications on LAN has been put out describing theoretical bases, standards, and current goals. /2,3,4,5,6,7,13/.—LAN developments initiated in 1985 primarily for 8-Bit BCs and known as ROLANET1 /1/ proved to be of limited or no use in the production of these computers. This was primarily because the rate of device production increased rapidly in order to meet demand, leaving little or no time for what was no doubt necessary additional componentry.—Based on positive international experiences, the quasi-LAN SCOMLAN was developed and implemented for the PC-1715 /14/. Users also found other solutions for the PC-1715 that became important for individual research institutions or collective combines /12,13/.—The ROLANET1 line was pursued for the 16-Bit PCs A-1759 and EC-1834, but was only partially successful due to the lack of a LAN adapter for the A-7150. The necessary hardware components were developed and adopted for the EC-1834 and have been produced since January 1989 (LAN adapter card K-8625, Transceiver K-8601, transceiver cable to connect the LAN adapter with the transceiver, 75 Ohm coaxial cable).—At the same time, alongside continued work on ROLANET1 software, whose goals are presented in /8/, the EC-NET software package was being developed in the Karl-Marx-Stadt Accounting Machine Factory. This occurred for several reasons:—ROLANET1 is oriented on a heterogeneous net structure, which takes into account not only 16-Bit PCs, but also 8-Bit PCs and other types of computers. In this way, the least powerful computer (the 8-Bit PC) essentially determines the system management.—Homogeneous nets composed of 16-Bit PCs rank higher and are necessarily equipped with Standard Gateway to ESER-EDVA in the form of the EC-7920 or IBM-3780 emulation.—ROLANET1 still is not suitable for working with data bank systems (e.g. REDABAS 4). This is a serious drawback, as rapid in-depth efficiency is possible only with data bank software.—Based on material resources, Robotron markets PCs based on available inventory, and LANs are currently not delivered as systems, but in the form of add-ons (a LAN adapter, transceiver, cable, software on diskettes, and documentation for each PC). Marketing is carried out by Robotron Berlin's Potsdam office. Documentation can also be obtained from the application center of Robotron's Accounting Machine Factory in Karl-Marx-Stadt.

In summary, ROLANET1 includes:—hardware components of various BC, PC, and EDVA, characterized by a transmission speed of 500 Bits/s; and—a software solution for heterogeneously structured nets.

EC-NET is a software package that was developed for nets of EC-1834s or its successors and that uses ROLANET1 hardware (500 Bits/s).

ROLANET2, which has also been mentioned in publications /10, 11/, includes:—hardware and software components of the K-1840 family and its successors. The hardware is characterized by the ETHERNET standards with a transmission speed of 10 MBit/s.—hardware components of the PC EC-183x family.

Building on this hardware, the development of ROLANET2 and EC-NET software for the EC-183x was two-pronged:—EC-NET successors; and—LAN software to meet increased demands for convenience and data security.

At the same time, LAN software was developed that will guarantee the use of the EC-1834 in the main operating systems of computers in nets under the K-1840 or its successors, as well as in nets under MUTOS.

These development trends will be discussed in further detail later.

Subsequently, the EC-NET software package is presented in a special way: After a brief description of the technical parameters, an attempt will be made to provide the interested reader with an overview of the performance spectrum by explaining selected commands.

EC-NET

EC-NET was designed to be a homogeneous local net, i.e., only the EC-1834 16-Bit computer and its successor can be connected to it. This means that user interfaces were established, as is the common international practice for computers of this performance class.

Hardware

Topologically, the EC-NET local net is constructed as a line bus and consists of the following hardware components:—K-8625 local net controller (network interface unit = NIU);—K-8601 transceiver (medium access unit = MAU) and transceiver cable; and—75 Ohm coaxial cable.

The local net controller is an intelligent interface card integrated into the EC-1834 computer. It accomplishes the data exchange between the computer bus and the transceiver. The main part of the controller is an 8-Bit computer consisting of a UA880 microprocessor, a 64 KByte RAM as program and buffer memory, and a

UA856 SIO-circuit for serial data input and output. The controller occupies one of the eight slots in the EC-1834's expansion unit.

The controller is connected to the transceiver by means of the transceiver cable, which can have a maximum length of 50 m (delivery standard 5 m). The transceiver is an independent container component. Its power supply comes from the controller via the transceiver cable. The task of the transceiver is to provide a link to the coaxial cable. The coaxial cable provides the common transmission medium and links the transceivers of all connected computers.

The stochastic CSMA/CD process (carrier sense multiple access/collision detection) is used to access the common transmission medium. The data transmission rate is 500 KBit/s and occurs as a base band transmission with manchester coding. Territorial reach is determined by the coaxial cable's length of no more than 1,000 m and the theoretically 255 connectable computers. In practice, a maximum of 12 PCs is recommended.

Software

The EC-NET program package is offered under the DCP 3.30 operating system. In addition to its own network program with NETBIOS, it includes components for installing the network program on a diskette or hard disk and for initiating the local net.

Physical access to the local net is achieved via the NETBIOS program after the program has been loaded into the main memory. This is done by calling up the program (e.g., A:/NETBIOS), after which the NETBIOS interface is available for application programs and can be used by them by triggering a software-interrupt with a vector of 5CH. Useful functions are those that establish connections, send and receive information, break connections, and provide status, all of which ensure secure data transmission. Connections are established using logic names that are allocated to the individual stations. Up to 16 names can be allocated to each station and used to establish connections. One station can operate a maximum of 32 connections.

The network program and its components build on and use the NETBIOS functions. Existing user interfaces are expanded and new ones are created by means of the network program. This applies particularly to diskette-related DOS functions, which can also be used in the network. The network program must be initiated for these functions to become available.

Initiation, as well as the other functions of the network, can be implemented either with the program menus or with the network commands. When working with menus, submenus lead the user to the function he plans to execute. In addition, every menu has a corresponding help file. The experienced user will prefer the network commands, which operate more quickly and are very similar to the DCP commands.

When a network program is initiated, every computer is given a computer name, checking that this name is not already being used by another computer. In addition, it is necessary to determine the scope of the computer's function within the network, for which the user can choose one of the four basic configurations shown in the table below.

Basic Functions in the Net

Configuration	Available Functions	Memory Requirement (including DCP)
REDIRECTOR	Sending information use of network diskettes dictionaries and printers	approximately 128 KByte
RECEIVER	Receipt and storage of information + REDIRECTOR	approximately 192 KByte
MESSENGER	Transmission of information between PC & RECEIVER	approximately 256 KByte
SERVER	Provision of diskettes dictionaries and printers for common use in the local net and MESSENGER	approximately 312 KByte

There should be at least one computer in each net whose hard disk or printer can be used by the other computers. In other words, at least one computer must be configured as a SERVER. This computer *must* have access to a hard disk drive. The functional scope of this PC is distinctive primarily in regard to receiving information. The use of network diskettes, dictionaries, and printers is possible with all configurations.

The following examples will give only network commands. All the examples can also be performed using menu functions.—For a computer acting as SERVER and receiving the name EC1, input the following command: C:(backslash)> NET START SERVER EC1;—For a computer addressed as EC2 and acting as MESSENGER, input the following command: C:(backslash)> NET SHARE PROG=C:PROGRAM/R;—After the network program has been initiated, this command remains resident in the main memory and is constantly active in the background. The user must specify which network diskettes, dictionaries, and printers he wishes to use or make available to the other computers if he is acting as SERVER.—Programs in the C:(backslash)PROGRAM dictionary and other dictionaries on the hard disk and printer of the EC1 computer should be made available to the other computers. However, the other computers should, for example, only be

able to read the programs. Several commands are required to achieve all these things:

1. Providing the dictionary

C:(backslash)> NET SHARE EC2P=C:USER (backslash) EC2/RWC This makes the dictionary C:(backslash)PROGRAM available to the other computers with read access rights (/R) under the short name PROG. If they wish to use the dictionary, they need give only the short name and not the complete path name.

2. Providing other dictionaries

The user of the SERVER computer has set up dictionaries for private use (e.g. C:(backslash)USER/EC2, C:(backslash)USER/EC3, etc.) for the other computers (e.g. EC2, EC3, etc.). These dictionaries should also be made available, protecting them from unauthorized use with a password. The following command is input for this: C:(backslash)> NET SHARE EC2P=C:(backslash)USER(backslash)EC2/RWC PRIVATE EC1

With this command, the dictionary C:(backslash)USER(backslash)EC2 is made available under the short name EC2P while limiting the access rights ((backslash)RWC = read, write, create, delete data). The password, PRIVATE EC2, must be given when the dictionary is used.

3. Providing the LPT1 printer

The printer should be made available under the short name NPRINT: C:(backslash)> NET SHARE NPRINT=LPT1 The user of computer EC2 wishes to use the dictionaries or printers provided by computer EC1 for general use. To do so he must input the following commands:

1. A:(backslash)> NET USE E: (backslash) (backslash) EC1(backslash)PROG This uses the dictionary of computer EC1, which has the short name PROG. This dictionary is addressed by computer EC2 as drive E, i.e., computer EC2 now has an additional logic drive at his disposal. However, in accordance with the granted access rights, he can only read this drive.

2. A:(backslash)>NET USE F: (backslash)(backslash) EC1(backslash)EC2P PRIVATE EC2 After this command has been implemented, the corresponding dictionary of computer EC1 can be used for private use as drive F. The password must also be given here. The user has both read and write access rights for this drive, meaning that he can read, change, or delete existing data or add new data.

3. A:(backslash)> NET USE LPT1 (backslash)(backslash) EC1(backslash)NPRINT This command allows use of the printer connected to computer EC1. This printer is addressed by computer EC2 as LPT1 or PRN.

Thus, the user of computer EC2 has at his disposal not only his own disk drives A and B, but also the network disk drives E and F and the network printer LPT1.

At the present time, the *current* network configuration of the network program can be stored with a menu function. The corresponding network commands are written into the file AUTOEXEC.BAT, so that each time the computer is turned on or rebooted the network program is automatically initiated and can be used with the same configuration. The original file AUTOEXEC.BAT is called up in AUTOUSER.BAT and at the end of the new file. For computer EC2 in the above example, the file AUTOEXEC.BAT would have contained at least the following: NET START MSG EC2 NET USE E: (backslash)(backslash)EC1(backslash)PROG NET USE F: (backslash)(backslash)EC1(backslash)EC2P * NET USE LPT1 (backslash)(backslash)EC1(backslash) NPRINT AUTOUSER (MSG in the first line is equivalent to MESSENGER. The asterisk '*' in the third line means that the operator is asked to input the password when implementing the command.)

The user can also work as usual with the additional logic drives or with the printer. This means that the normal DCP commands (such as DIR, COPY, PRINT, etc.) can still be used.

In addition, integrating the virtual diskette system and other network components into the operating system makes it possible to access these additional logic devices with many programming methods. These include both programming languages (Assembler, PASCAL, T-PASCAL, C, etc.) and standard packages (such as data bank systems like REDABAS4 and others). Joint data use by several network participants is also possible. This is supported by, for instance, the granting of access rights, file locking (temporary locking of a file to other users), and record locking (temporary locking of individual data sets to other users).

Independent of this system, the operator can also communicate by receiving information and then sending it to one or all of the connected computers. Depending on the scope of the functions given when the network program is initiated, incoming information can be read, printed out, stored in the main memory, or stored in a file and read later.

The local net EC-NET was developed by the Robotron Accounting Machine Factory in Karl-Marx-Stadt and can be added on to already installed and operational EC-1834 computers. This net has been used in the GDR since November 1989.

From the standpoint of technical parameters, the local net EC-NET is an intermediate class LAN. It is a homogeneous net, because only the EC-1834 computer and its successors are included. This has advantages not only in customer service, but also in using the net, because all connected computers have the same access capabilities and user interfaces to the net. The user interfaces are equivalent to the international norm for computers of this performance class. They also allow users who have little knowledge of local nets to use EC-NET.

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MICROELECTRONICS

Development Tempo of Bulgarian Microelectronics Increasing

90CW0123 East Berlin AUSSENWIRTSCHAFT in German 29 Nov 89 p 41

[Article: "People's Republic of Bulgaria: High Tempo of Development in Electronics"]

[Text] In the restructuring and technological retooling of the Bulgarian economy, electronics is assuming a leading role. Thus, in 1988 this production complex alone was responsible for 30.6 percent of the total increase in the country's industrial production, amounting to 5.1 percent, or 2.4 billion leva. The basis for this, in addition to an above-average rate of increase in labor productivity for the sector of 9.7 (overall 8.9) percent, was an 18-percent increase in the output of electronic products (1987: 16 percent) to 5.8 billion leva. Of this, 1.7 billion leva or 29.9 percent was attributed to new or enhanced products.

Developmental Emphases and Orientation

Both in 1989 and beyond, electronics will assume the leading role in the structural modification of industry. This year, manufacturing of electronics and information systems is expected to increase especially quickly to reach a 22-percent share of the total output of electronics products.

With the extremely high tempo within the sector and in Bulgarian mechanical engineering as a whole, the manufacture of technical equipment for microelectronics is to be developed. In this area, Bulgaria is cooperating closely with Soviet organizations.

The strategic development of the sector is taking into account the needs of the Bulgarian national economy as well as the development of electronics and data processing in the other socialist countries, primarily within the framework of the Comprehensive Program for Scientific-Technical Progress in the CEMA countries through the year 2000.

In this connection, for example, a comprehensive renovation of the peripheral memory production project is planned. (Bulgaria has specialized in this field within CEMA.) The removable disk devices produced to date are gradually being replaced by hard disks. Hard disks with a capacity of 10, 20, 31, 121, 317, and 635 MB are already being offered. Within the next 1 to 2 years, production of 300- to 600-MB hard disks should begin.

Also, a program is being implemented for development and manufacture of optical WORM memories, including compact disks for entertainment electronics. Also planned is the development of erasable and rewritable optical memories. To this end, Bulgaria is striving to increase cooperation with foreign partners.

In the microelectronics area, the plan is to increase production of integrated circuits 1.6-fold in 1989 as compared to 1988 and 3-fold by 1990. The use of technologies and equipment for production of 256-Kbit and 1-Mbit memory chips and 16- and 32-bit processors is also to be pushed.

For example, at the beginning of this year, the Combine for Microelectronics Botevgrad introduced the 16-bit microprocessor system SM688, compatible with the Intelsystem 8088.

Production of active and passive components for SMD assembly is currently being prepared for.

The express goal of the Bulgarian components industry is to cover a total of 55 percent of the demand for active components and 85 percent of that for passive components from domestic production by about 1990.

In this connection, a significant expansion of production capacity is also underway. Thus, at about the beginning of 1989, a new printed circuit board plant began operation in Pravez. It is part of the Combine for Microprocessor Technology Pravez and, in the first stage of the project, will meet the combine's demand for printed circuit boards. By the end of 1990, it should reach full capacity and use only CAD/CAM technology for development and production.

Within the framework of the industrial synthesis of single silicon crystals with diameters up to 200 mm and a mass of 60 kg, scientists at the Bulgarian Institute for Solids, working with the Soviet physico-technical Joffe Institute, developed a special system with which substrates with ideal surfaces for microelectronic integrated circuits are obtained. To develop these technologies and begin their production, an international laboratory has been created in Plovdiv. Before the end of this year, a production plant for highest purity crystals for electronics is to begin operation.

In the area of microprocessor technology, the greatest growth rates are planned for systems based on the personal computers (PC's) and microcomputers produced at Pravez.

Thus, among other things, the Combine for Microprocessor Technology Pravez introduced its first 32-bit PC, the Pravez 386, as a desktop model at the 44th International Trade Fair Plovdiv '88. It is based on the 80386 processor, which can be expanded using a 80287 or a 80387 coprocessor. The 1-MB-RAM can be expanded to 10 MB. The ROM has a 128-KB capacity.

The 16-bit computers in series production at Pravez have a 640-KB storage capacity. Both diskette and hard disk technology are used for data storage.

Much attention is being directed to the networking potentials of computers in local area networks (LANs). For example, at the show organized jointly with Isotimpex in February of this year in Berlin, the Pravez Combine offered 5 LAN's, including the mircoring LAN MicroSTAR. MicroSTAR has star configuration and permits connection of 8 PCs to the central node. Successful work is also being done on the development of computer networking systems with the relevant systems software. Offerings include microprocessor systems for education and training, health services, the building industry, production and control management systems all the way to expert systems such as Cortech, a system for the control of technological processes, and Agrotech, an expert system for agrarian technologies.

In the array processor field, the Bulgarian firm Incmos occupies a leading position among the socialist countries. The array processors currently offered by Incmos have a performance rate of 12 million floating decimal operations per second. Production of a new model with increased performance and a smaller footprint as well as array processors for minis and micros is in preparation.

Currently, systems are being produced by Incmos using minicomputers, array processors, and specialized software, with which performances of 100 million operations per second (MIPS [million instructions per second]) are obtained. Work is underway to achieve a performance of 500 MIPS by year's end.

Overall, the objective of the Bulgarian microelectronics industry is unmistakably to provide increasingly complete user solutions. A key position in this is occupied by the Enterprise for Software Products and Systems (SPS) with approximately 1,500 employees. In cooperation with other partner companies, SPS is undertaking development of client-specific hardware and software solutions. At the Plovdiv '88 Trade Fair alone, SPS's offerings consisted of more than 180 displays, including 172 program solutions.

Other dynamically developing areas of the Bulgarian electronics industry are optoelectronics and laser technology. Laser technology production should increase in 1989 by more than 70 percent over the preceding year. In 1989 alone, approximately 460 laser systems are to be installed, including 380 in the health field, 66 in industry, and 10 in the building industry.

Bulgaria has increasing capacity in the optoelectronics field, especially for optical fiber and cable intended primarily for the production of fiber optic connection systems, devices, and components for communications electronics.

GDR: ASIC Design Center of VEB Carl Zeiss JENA Profiled

90CW0121A East Berlin NACHRICHTENTECHNIK-ELEKTRONIK in German No 1, Jan 1990 pp 15-17

[Article by F. Grunert, KDT, H. Muller, KDT, A. Wohlrab, Jena: "Bulletin from the VEB Carl Zeiss Jena Collective Combine"]

[Text] The ratio of application-specific integrated circuits (ASICs) has exhibited greater than proportional growth in the semiconductor market with respect to other electronic components since the beginning of the 80's. Among these, the gate-array and standard cell circuits are particularly prominent.

The specific features of these components is that the device manufacturer can use components that are quick and inexpensive to develop. This is because of the high degree of standardization in the component configuration on the chip (gate array) and/or of the design software (standard cell).

Operating an internal ASIC development department requires, in addition to the qualification of employees, a high investment in design computer technology and software. These can only be justified if a specific number of ASICs must be designed continuously year after year.

For this reason, the basis for constructing an ASIC Design Center can only be a long-term product strategy utilized to forecast the future use of ASICs.

The device developer does not automatically recognize the necessity of using ASICs. A lack of data, high initial cost and a lack of trust in the data created during the CAD process oppose the introduction of ASICs in the device development process. Additional inhibiting factors are the high cost of preparing samples, the requirement of a correct initial design, the SMD housing having a large number of pins but a small pin grid and the use of previously unutilized, by the device developer, test methods for testing the ASIC. Such methods include, for example, the LSSD test (Level Sensitive Scan Design).

In particular among these points of view, special importance is attached to the structure of an ASIC Design Center as a support resource providing know-how. The work of this center has a decisive effect on the speed and effectiveness with which ASICs in the application area of the Design Center are introduced into the device development processes.

The possibility of utilizing this knowledge is supported by the publications [1] [2].

1. Tasks of the ASIC Design Center Jena

The ASIC Design Center Jena was structured with the objective of creating a central location for ASIC design and application for the VEB Carl Zeiss JENA Collective Combine. This center, in accordance with its leadership role, is to insure uniform ASIC know-how for all development areas. This task does not run counter to the tasks of the ZMD Collective Combine as the developer of ASIC systems and producer of ASICs, but rater creates the prerequisite for an effective division of labor between the semiconductor manufacturer and the device developer.

In its over 40 ASIC designs so far, the Design Center Jena uses exclusively the ASIC systems of the ZMD Collective Combine. This decision was made from a technical point of view based on the requirement for exclusive integration of digital functions using the following evaluation criteria:

- Universal application of computer-aided design
- High degree of integration and low power consumption
- Quality-control support of the ASIC at the manufacturer's
- Automatic generation of the test set with a high degree of depth (LSSD test)
- Assurance of design (simulation of the intended design, dynamic simulation)
- The potential for using the ASIC test interface for the circuit- board test
- Design cost and production cost/gate function.

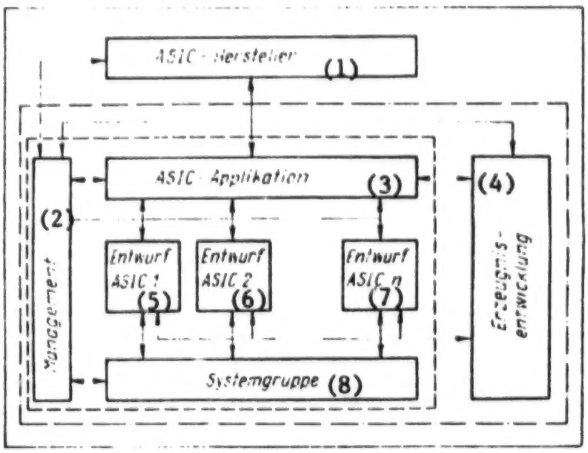
To insure a universal circuit-board test strategy and to avoid additional development expenditure for the functional testing (hardware and software), only circuits that can be tested using LSSD have been designed to date and the potential of the LSSD testing within the U1600S system required.

Other ASIC systems of the GDR (e.g. the digital ISA system) were able to satisfy the aforementioned criteria only partially or not at all. They were rejected for use in the Design Center. The integration of analog functions, which has not been possible to date in the ASIC systems used, is implemented in part using hybrid integration or the use of digital function principles. For cost reasons, this choice is the better solution.

The development of analog ASICs based on the ISA system is not absolutely impossible for exceptional cases having technical or economical reasons.

Within the framework of the aforementioned boundaries, the ASIC Design Center Jena has the following tasks:

- The execution of contract designs for product development areas or following-through on internal designs of product-areas.
- Assuring a defined interface for all development areas in the R & D requirements acquisition areas. The transfer of ASIC designs, CAD software and hardware requirements to the ASIC systems. Classification of sample preparations. Acceptance of sample circuits, etc., from circuit manufacturers.
- Making available and maintaining the CAD tools for logic synthesis and ASIC design including the training of product developers in the application of the CAD tools for the actual tasks they have to solve.
- The expansion and maintenance of the design database by building and constantly updating the software macro library and adapting these to the further developed ASIC systems.
- Preparation of guidelines for further work in the area of the use and design of ASICs, and computer-aided circuit and logic design.
- Determination of broad-based tasks for ASICs with regard to circuit-board use, the processing in hybrid circuits as well as the utilization of the potential in the ASIC test interface for testing in following processing stages.
- Consulting and cooperation in electronic designs with the goal of effective and broad use of ASICs, and providing a new technological level of development and manufacturing for electronic modules.
- Acquisition and systematic classification of hardware/software requirements of the product development department for ASIC systems and compelling the use of these by ASIC manufacturers.
- Assurance of application tasks or contacts to other design centers, documentation management, follow-on utilization concerns, sample testing and dissemination of data.
- Assurance of the design computer technology and data transfer concepts in cooperation with product development and the ASIC manufacturer.
- Organizational guidance of the ASIC designs from the statement of the task to the Technical Delivery and Acceptance Conditions (TLAB).



Key:—1. ASIC manufacturer—2. Management—3. ASIC application—4. Product development—5. Design ASIC 1—6. Design ASIC 2—7. Design ASIC n—8. Systems Group

2. Structure and Work Organization

The structure and work organization chart of the ASIC Design Center result from the aforementioned tasks (Figure 1). Previous experience has shown that the following subdivisions represent the optimal choice for solving these tasks:

- Design group
- Systems group
- Applications group.

The design groups are organized according to the product. When selecting the design group leaders, the long-term orientation of these people toward specific product lines is used as a selection criterion. The reformation of the design group at the beginning of a design task while retaining the design group leader responsible for the product proved to be a good decision with regard to the exchange of experience and raising the level of knowledge within the ASIC Design Center. In this manner, good communication relationships were created particularly at the interface between the product developer (system knowledge) and the ASIC designer (design knowledge).

Separating the design into separate areas according to the ASIC types was rejected as unworkable.

The applications department currently handles all tasks resulting from the defined interfaces between the device developer, circuit-board department, the hybrid circuit development department and the design department or the manufacturer of the ASICs. In the future, the intention is to expand the area of this tasks to include follow-up of internal designs in the product groups. At this time, this task is handled by the design groups. This also includes performing qualification tests and processing requirements for subsequent utilization.

The system group, in addition to maintaining design software and data management processes, implements tasks for internal rationalization of the processes in the Design Center. They prepare conceptual tasks with regard to the basis of design computer technology, software concepts and data transfer tasks.

Linking employees of the system groups into the design group proved a success for the total process in the phase of prototype designs and when introducing new design system.

3. Interface to the Device Development Department

The work of the Design Center is regulated by company guidelines. The device developer can, as a function of his state of qualification, avail himself of the following entry points for implementing his ASIC development project:

3.1. Problem Statement This interface lies at a very early time in the device development process. The product developer still does not have a final concept for solving the required function. The ASIC designer has a decisive say in the system concept of the electronics. In this respect, he must possess a high degree of creativity and knowledge of the device. ASIC designs using this interface almost always are accompanied by the advantage of providing a total solution that is easy to integrate. This solution may comprise one or more ASICs, depending upon the size of the problem. The complex solution of the posed development task using ASICs allows the maximum possible verification of the system idea by simulating the compound circuit. The long development times, the high requirement of computer time and the steep learning curve in a device concept during the ASIC design are disadvantages. Examples for such solutions are the circuit groups U5201 FC-304, FC-305, FC-308 (measurement systems): U5301 FC-308, FC-312 (digital image processing) and U16216 FC-301, FC- 302 (digital interpolator).

3.2. System Design This interface is based on a firm system concept by the product developer. Within this concept, the modules intended for integration within an ASIC are described functionally but represent a "black box" in circuit terms. The design requirements are transferred as a statement of a task. The main components of this statement of the task, in addition to commercial data available at the time, are:

- Function description
- Test strategy
- Block diagram
- Pin list
- Proposed symbol
- Required conditions of operation
- Special requirements (driver power, expanded operated conditions)
- Required limits (dynamic, static).

This interface represents the main entry point of the product developer for a contract design in the ASIC Design Center.

3.3. Module Design The transfer of module designs up to and including the total circuit of the ASIC together with the test strategy and the command files for technological final processing (layout, dynamic simulation, generation of the test set) presumes, to the maximum extent, that the product developer provides his own design. This method of operation presents itself when designing gate arrays of the U5300 system. This system makes it possible for the product developer to rapidly convert his idea "in situ" without restrictions regarding material acquisition, etc. Losses in time and data, such as those that always occur during a contract development job, are almost completely eliminated. This mode of operation is supported by the availability of design systems that can be run on XT-compatible PCs (PC-GAT, MELGET). The systems have an interface (NBS) capable of passing data to the gate-array design system ARCHIMEDES.

The samples are tested after the sample circuits are provided by the manufacturer (ZMD). This testing is the responsibility of the product developer. In the event a problem occurs, the Design Center provides support by resimulating functions suspected of containing errors. This pattern can then be used as a static functional test together with the use of suitable test systems. After sample testing is completed, the product developer is obligated to inform the Design Center of the result achieved. He must also sign the TLAB as the final point in ASIC development when the test results are positive. At that time, the following data must be provided as a cooperative effort between the ASIC Design Center and the product developer:

- The documentation of the ASIC contains:

—Symbol

—Block diagram

—Pin list

—Housing drawing

—Functional description

—Application example

—Limits (general, customer-specific)

—Handling specification.

- The design data contain

—Data memory with the placed/laid-out ASIC

—A record of the design procedure

—Command files

—A command file implementing automatic processing of the entire design

—A record for simulating the dynamic-critical path

—A record containing NBS texts

—The LSSD test set

—Testability analysis

—Test report

—TLAB

—Commercial information (requirement development, expenditure analysis, etc.)

—Miscellaneous (e.g. a decision for redesign).

The process is guided organizationally by a hierarchical system of milestones. At these milestones, the state of implementation of fixed tasks are to be shown.

The main items in the development process are represented by the defense of the system design, the defense of the design results (transfer data set to the manufacturer) and the final defense following sample testing.

4. Results

The ASIC Design Center started operation in 1986. To date, 14 ASICs were designed in the U5200 system, 26 ASICs in the U5300 system and 3 ASICs in the U1600 system. Table 1 provides an overview of ASICs having large variety of applications.

Table 1 ASICs with a Number of Different Uses

Serial Number	Type	Function
1	U5201/ FC114	Programmable 8-bit
2	U5201/ FC302	Interface for serial microcomputer connection and stepper motor control
3	U5201/FC307	Dual high-speed 22-bit counter and adder with parallel data output
4	U5201/FC309	Hex stepper motor control with computer interface
5	U5201/FC310	Differential characterizer
6	U5201/FC311	4x24-bit RAM with control logic
7	U5201/FC312	Programmable measurement interface for incremental measuring system having 4/8-bit interface for U8047/U880
8	U5301/FC301	Dual interface channels for incremental
9	U5301, FC302	Driver for 4 CCD lines with controller (can be cascaded)
10	U5301, FC303	Dual interface channels for incremental sensors with 26-bit binary counter, RAMs adder, 27- bit parallel output that can be connected to a 16-bit bus
11	U5301, FC304	Network controller for 16-bit systems (MMS 16 field bus)
12	U5301, FC305	PIO with programmable data width and number of channels with 2 memory planes

Table 1 ASICs with a Number of Different Uses (Continued)

Serial Number	Type	Function
13	U5301, FC307	ALU (4xSN74181 and 8xS3002), can be cascaded, with memory block (11x16-bit)
14	U5301, FC309	Interface for serial microcomputer connection and stepper motor control
15	U1626, FC002	Interface circuit for translational and rotational distance measuring systems with measured-valued interpolation, 32-bit parallel output, serial interface

The growth of gate functions designed per designer and time unit can be proven statistically. The causes can be found primarily in the use of previously prepared software macros and an increasing level of qualification as well as the organizational regime. The design computer technology (K1840) sets technical limits in design effectiveness in particular when designing ASICs in the U1600 system. Figure 2 shows the current design computer base. Using the previous circuits, it can be proven that all circuits have a high degree of repeat modules. The use of elements from the software macro library, beginning as early as the system design phase, counteracts the multiple design of functionally identical or similar modules.

Within the framework of the work done to date, a software macro catalog was create d. The functional repertoire of this catalog did not make use of standard circuit series. This catalog continues to be updated in the continuing work.

The improved technical parameters and increased scope of integration of the U5300/U1600 Systems results in a pronounced enlargement in the application areas for ASICs. This fact will be reflected in an increased type diversity, compared to the number of types developed on the U5200/U1500 Systems.

The coordination of similar functional requirements from various development areas or cooperative development efforts between different companies with regard to ASIC development plans is receiving increasing importance, in particular for economic reasons, with an increasing level of integration.

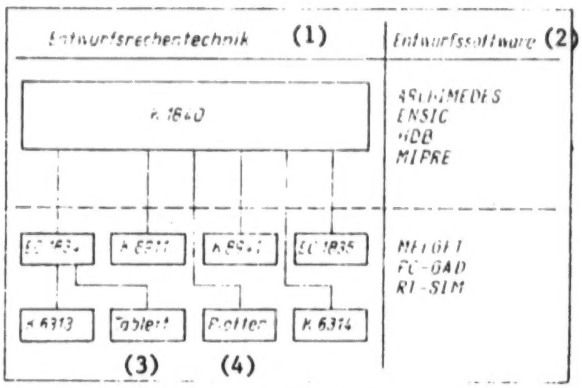


Figure 2. Design Computer Technology and Software Base

Key:—1. Design computer technology—2. Design software—3. Tablet—4. Plotter

The preparation of a follow-on utilization catalog is the first step in this direction.

5. Objectives for Continued Expansion of ASIC Use

In further work, in addition to ensuring up-date design requirements from product development, the rationalization of the work processes in the ASIC Design Center, internal qualification by means of prototype designs based on new ASIC systems, cooperation in the utilization of ASIC test interfaces for circuit-board test and the qualification of product developers to provide their own design using gate arrays are primary tasks. A main concern in technical work will be the computer-aided design of large digital electronic systems. In this work, the potential for modelling and simulating logic blocks at the register- transfer level should be investigated in particular.

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